ANNEX

Overview

As mentioned earlier in this book Gen3 offer a draft text for a new IPC test method for *Process Characterisation of Circuit Assemblies using SIR*. Currently IPC have two guidance documents for taking SIR measurements of electronic assemblies, and they are IPC 9202 - Material and Process Characterisation / Qualification Test Protocol for Assessing Electrochemical Performance, and IPC 9203 - Users Guide to IPC-9202 and the IPC-B-52 Standard Test Vehicle. These two documents need to be accompanied by a test method that should be in TM 650. To help the industry meet this gap Gen3 has drafted a test method that can be considered as the starting point as a IPC test method. This draft has been prepared by Graham Naisbitt and Dr Chris hunt. Graham is the current vice-chair of IPC 5-30 Cleaning and Coating Committee, and previously chair of the SIR committee. Graham also works with the IEC TC91 committee and is the maintenance leader for for SIR, CAF, ionic contamination testing, and solderability. Chris has championed many of the advances in SIR testing while at the National Physical Laboratory, and was chair of both the UK national committee and chair of IEC TC91.

While every effort has been made that this document is as complete as possible, it has not been possible to fully complete the document. Where Gen3 has not wished to make a statement, or where we are aware that the committee needs to look especially careful at the proposed text, we have appropriately marked it as such. It is expected that the IPC committee will make comments and amendments throughout the document.

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OBJECTIVE EVIDENCE

Process Characterisation of Circuit Assemblies using SIR

GEN3 Test Method: G3-2201

FOREWORD

The object of this Test Method is to assist in Characterising a Material Set used to assemble electronic assemblies. It is complementary to:

IPC 9202 - Material and Process Characterisation / Qualification Test Protocol for Assessing Electrochemical Performance

IPC 9203 - Users Guide to IPC-9202 and the IPC-B-52 Standard Test Vehicle

Subsequent use of this same Test Method can also be then used to Validate the chosen assembly process.

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1 SCOPE

This Process Characterisation Test measures and records changes in Insulation Resistance values under heat and humidity condition to help identify unwanted electro-chemical reactions on the surface of a representative example of an electronic circuit assembly that may adversely affect the reliabilityof the electronic end-product.

It quantifies any deleterious electro-chemical effects that may arise from flux or other process residues occurring with a selected material set.

It is based upon the use of the IPC B52 test coupon. This coupon is intended to be representative of the electronic circuits that are intended for the end-product and exhibiting the most likely entrapment zones within a typical assembly production process.

It is a quantitative not a qualitative test protocol.

For process materials such as fluxes, which may leave undesirable residues and hence require cleaning, the results obtained from the test will depend not only on the characteristics of the residue, but also on the effectiveness of the manufacturing / assembly cleaning operation.

The intent of this test is to show that a proposed manufacturing process or process change can produce hardware with acceptable end-item performance. These process changescan also involve a change in any one of the assembly production process. It can also pertain to a change in bare board supplier, solder mask or metallisation, soldering material supplier, conformal coating etc.. The test vehicle construction will vary depending upon which of these changes is being evaluated.

NOTE: 'This testing is a “site specific" qualification process using coupons that should be prepared at the users location, using the intended processes and equipment whenever possible. If this cannot be done, then care must be taken to ensure that the processed test coupons are kept free from any secondary contamination whilst in transit to test facility. The actual testing of the prepared coupons can then be done either at the users’ premises or at a suitable laboratory.

2 NORMATIVE REFERENCES

IEC 61189-5-501	General test methods for materials and assemblies – Surface insulation resistance (SIR) testing of solder fluxes
IEC 61189-5-502	General test methods for materials and assemblies – Surface Insulation Resistance (SIR) testing of assemblies
IEC 61189-5-504	General test methods for materials and assemblies – Process ionic contamination testing (PICT)
IEC TR 61189-5-506	General test methods for materials and assemblies - An intercomparison evaluation to implement the use of fine-pitch test structures for surface insulation resistance (SIR) testing of solder fluxes in accordance with IEC 61189-5-501
ISO 9455-17	Soft soldering fluxes — Test methods — Part 17: Surface insulation resistance comb test and electrochemical migration test of flux residues
ISO 5725-2	Accuracy (trueness and precision) of measurement methods and results — Part 2: Basic method for the determination of repeatability and reproducibility of a standard measurement method

IPC-J-STD-001	Requirements for Soldered Electrical and Electronic Assemblies
IPC 9201	Surface Insultation Resistance Handbook
IPC 9202	Material and Process Characterisation / Qualification Test Protocol for Assessing Electrochemical Performance
IPC 9203	Users Guide to IPC-9202 and the IPC-B-52 Standard Test Vehicle
IPC-TM-650 Method 2.6.3.7	Surface Insulation Resistance
IPC WP019B	An Overview on Global Change in Ionic Cleanliness Requirements

3 APPARATUS AND MATERIALS

3.1 Environmental Chamber

A damp heat chamber capable of programming environments of 20°C ± 2°C to 100 °C ± 2°C and relative humidity up to 93% with control of ± 3% at a specific RH setpoint.

The chamber should be constructed with stainless steel inner surfaces and be wellinsulated.

The temperature and humidity levels of the test chamber shall be recorded throughout the test. Supplementary Independent controllers may also be used.

It is essential to have adequate mixing of water vapour and to avoid condensation occurring elsewhere in the chamber than on or around the cooling and dehumidification coils.

The samples shall be kept above the dew point and be shielded from dripping or flying condensate that can occur near to the chamber door.

To ensure that there are no residues from previous tests, between every test run the chamber shall be cleaned down using de-ionised water and IPA solution and a lint free cloth.

3.2 Surface Insulation Resistance (SIR)Measurement system

The measurement system shall be comprised of a measuring device capable of measuring surface insulation resistance (SIR) in the range of at least $10^6\Omega$ to $10^{12}\Omega$.

A test and bias voltage supply capable of providing a variable voltage from 3V to 100V ± 1%

A 1 MΩ (10^6 Ω) current limiting resistor shall be used in each measurement channel.

The system shall be capable of individuallyselecting each test pattern under measurement.

The tolerance of the total measurement system shall be:

- ± 5% up to $10^{10}\Omega$ at 5V
- ± 10% between $10^{10}\Omega$ to $10^{11}\Omega$ at 5V
- ± 20% above $10^{11}\Omega$ at 5V

If a different test voltage is to be used, the measurement circuit shall be assessed at that voltage rather than the 5V stipulated.

The resistors used to confirm the total measurement system tolerance as shown above, shall have a tolerance of:

- ± 0.1% up to and including 10^6 Ω
- ± 1% above 10^6 Ω at up to and including 10^8 Ω
- ± 5% above 10^8 Ω and up to and including 10^{10} Ω
- ± 10% above 10^{10} Ω

The measurement system shall be verified by substituting a Resistor Verification Coupon (RVC) see section 3.6. This coupon shall use uncertified but "known value" resistors of

- 10^6 Ω ± 1%
- 10^7 Ω ± 1%
- 10^8 Ω ± 5%
- 10^9 Ω ± 10%

The data sampling rate shall be repeatable at not more than 20 minute intervals.

The GEN3 AutoSIR system has proven repeatability using the Gauge R&R methodology called out in ISO 5725-2 at 10%. *This reference is to an ISO document, IPC may prefer an alternative reference.*

3.3 Interconnection Connectors, Cablingand Test Cabling

Due to the extremely low levels of current involved in SIR measurement, it is important to prevent stray or unintended sources of current in the fixture or data acquisition system itself. Stray currents may include electromagnetic noise, leakage between wire insulations or channel-to-channel leakage in the data acquisition of the measurement system.

The recommended cabling is PTFE-insulated wire or cable.

3.4 Test Rack

It is recommended that test racks be used rather than the conventional use of hard wiringthat is both a significant potential for the introduction of contamination and hugely time consuming.

As the test rack will age in each test, it is recommended that the test rack be manufactured from electro-polished stainless steel.

Edge card connectors should have gold plated post/pin mating and bifurcated beam contacts suitable for the IPC B52 test coupon that has a thickness of 1,40 mm to 1,78 mm (0.055 to 0.070 inch), and capable of withstanding temperatures up to 105 °C.

See section 6 for more information. *This reference will need to be checked in the final version, as there may be a change in the numbering.*

3.5 Hard Wiring

If hard wiring is used in place of test racks:

For each coupon, first cover the patterns to be tested with aluminium foil to protect them from contamination during interconnect attachment soldering. Solder a PTFE-insulated wire to the appropriate coupon tab using a soldering iron and the flux-cored solder wire. Use a minimum amount of solder to make eachjoint and do not allow solder or flux to contaminate the test pattern. Tag each wire so that it can be identified outside the humidity chamber.

Cleaning solvent (where required). Use a solvent recommended by the flux manufactureras being suitable for the removal of post- soldering flux residues.

Flux-cored solder wire conforming to J Std 004B

3.6 Verification Coupon

Prior to every test an RVC (Resistor verification coupon) or "Checker Card" shall be used. This shall be fitted with non-certified but "known value" resistors of $10^6\,\Omega$; $10^7\,\Omega$; $10^8\,\Omega$ and $10^9\,\Omega$ resistors in specific current pathways per Figure 1.

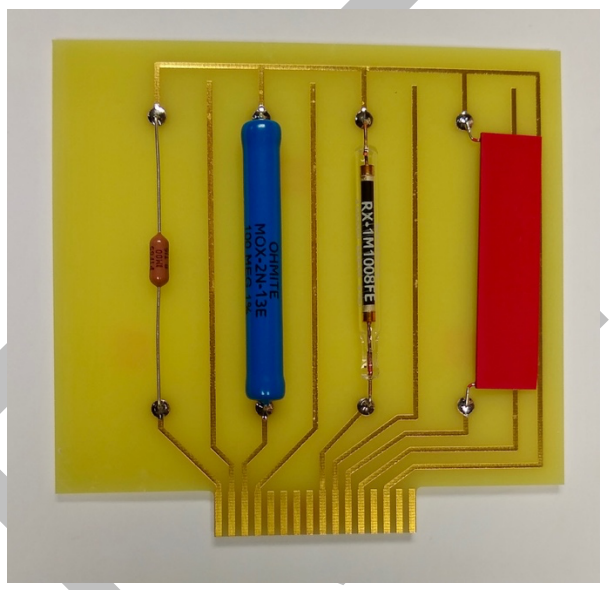

Figure 1: Checker Card example

The RVC or Checker Card should have a protective metal (stainless steel) cover attached with stainless hardware to the grounded mounting holes on the coupon to protect the resistors from contamination or damage during handling operations. See Figure 2.

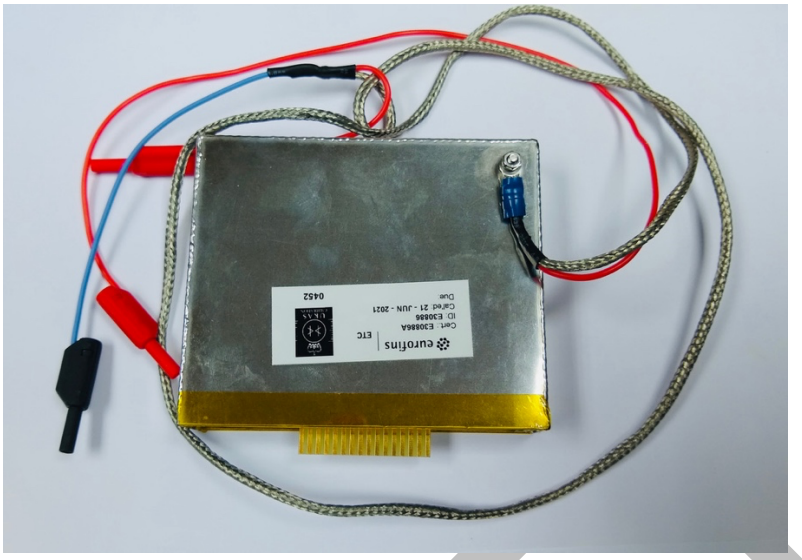

Figure 2: Checker Card in protective case

Calibration:

For system calibration, this coupon shall be fitted with certified, known value resistors, shown below and certificated by NIST certified laboratory:

- 10^6 Ω
- 10^8 Ω
- 10^{10} Ω
- 10^{12} Ω

4 TEST COUPONS

4.1 IPC B52

The B52 test coupons shall represent the substrate materials, assembly materials and fabrication processes intended for production.

The bare coupon shall be manufactured by the intended supplier or AABUS.

True Dummy Components shall be used as representative of the intended production assembly. As the test pattern is used to monitor the effect of the chosen material set, they must be exposed to all the intended assembly processes.

Prior to being subjected to conditioning the components are soldered onto the board, usingmethodologies replicating, as closely as possible, the proposed production techniques.

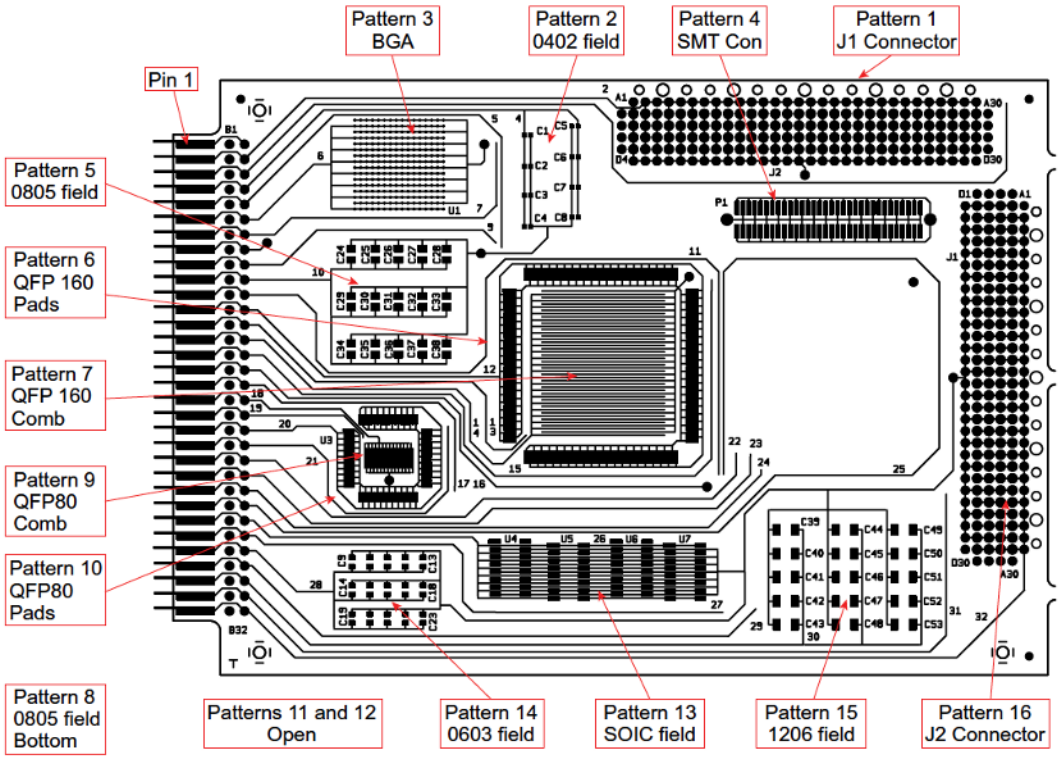

Figure 3: IPC-B-52 Top Side – Main SIR Board Patterns. Ref: IPC-9202-3-1

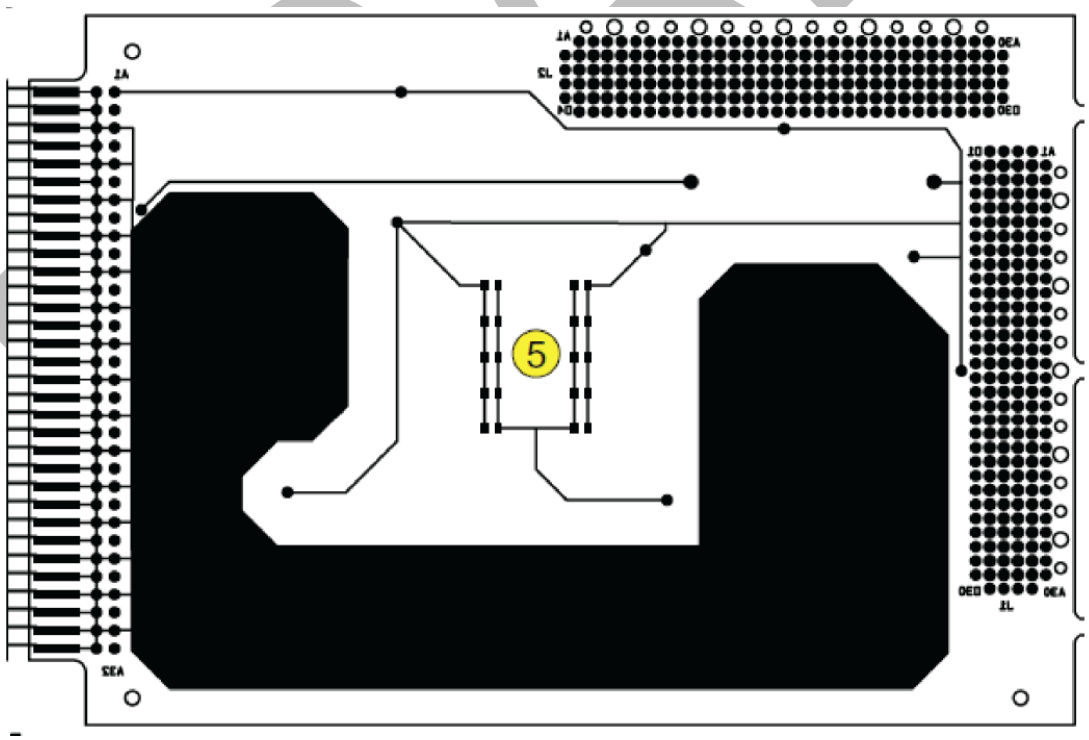

Figure 4: IPC-B-52 Bottom side

4.1.1 B52 Bill of Materials

Table 1: IPC-B-52 Bill of Materials

ID	Component/Pattern	Qty	Component Details
1	TH connector 4 × 24 pins	2	AMP part 536501-3 or equivalent.
2	Capacitor, 1 pF to 10 pF, 0402 package	8	Surface mount ceramic capacitor, 0402 body, 1 pF to 10 pF, DC 50 V , 5 % tolerance. AVX part 04025A100JAT2A or equivalent.
3	BGA, 256 IO, 1 mm pitch, isolated	1	Dummy component, no internal die or wires BGA, 256 I/O, full 16 x 16 array, 1,0 mm pitch, 17 mm body size.
4	SM connector IEEE 1386, 2 x 16 pins	1	Molex Waldom part 71436-2164 or equivalent.
5	Capacitor, 1 pF to 10 pF, 0805 package	25	Surface mount ceramic capacitor, 0805 body, 1 pF to 10pF, DC 100 V , 5 % tolerance. AVX part 08051A100JAT9A or equivalent.
6	QFP160 0,65 mm pitch, isolated	1	Dummy component, no internal die or wires, quad flat pack, 160 I/O, 28 mm square body, 0,65 mm pitch.
7	QFP80 0,5 mm pitch, isolated	1	Dummy component, no internal die or wires, quad flat pack, 80 I/O, 12mm square body, 0,5 mm pitch, 2 mm lead footprint.
8	Capacitor, 1 pF to 10 pF, 0603 package	15	Surface mount ceramic capacitor, 0603 body, 1 pF to 10 pF, DC 50 V , 5 % tolerance. AVX part 0603A100JAT2A or equivalent.
9	SOIC16, 1,27 mm pitch, isolated	4	Dummy component, no internal die or wires, small outline integrated circuit, 16 I/O, 1,27 mm pitch leads, 3,8 mm body.
10	Capacitor, 1 pF to 10 pF, 1206 package	15	Surface mount ceramic capacitor, 1206 body, 1 pF to 10 pF, DC 100 V, 5 % tolerance. AVX part 12062A100JAT92 or equivalent.

4.2 Alternative test coupons

If the user intends to use a test coupon other than the IPC B52, it is recommended that the user refers to the IPC 9201 SIR Test Handbook, Section 3.3.8 that deals with important design considerations.

5 PROCESSING THE COUPONS

The process materials: adhesives, flux, paste,underfill, coating etc., must be the same materials as intended for use in production.

Once the coupons have been processed, it is essential that they be transferred to the test chamber as soon as practicable. During this time, they must be kept away from sources of random contamination that might compromisethe test results. ESD safe suitable bags should be used for each processed coupon.

5.1 Sample Identification

Test coupons shall be identified using a positive, permanent, and non-contaminatingidentification method.

5.2 Sample Size

It is suggested that to determine the electro chemical compatibility of the intended material set, a minimum of 3 vehicles should be tested for each material/process combination. This sample size was

calculated by setting a “consumers risk”' at 10% (confidence of 90%).A complete explanation of how this sample size was determined can be found in IPC-TR-467. *The reference to TR-467 needs to be verified.*

It is recommended that an additional unprocessed coupon be tested as a control. It is suggested that a minimum of 3 test coupons plus 1 control, be used at each separate assembly process stage.

By this method, it will be convenient to identify which process step might have initiated an unacceptable SIR result, or where there has been a distinctive drop in the measurements.

The B52 coupon has 16 individual test sites so, as an example, the test matrix might comprise:

- Bare copper coupon – 1
- Coupon + Surface finish and permanent Solder Mask – 3
- Surface Mount Adhesive – 3
- Coupon + Solder Paste – 3
- Coupon + Underfill – 3
- Coupon + Conformal Coating – 3
- Total = 1 + 3 + 3 + 3 + 3 + 3 = 16 coupons

Therefore, 16 x 16 test channels = 256 test channels

5.3 Sample Preparation

The sample manufacturing process used in this method is assumed to replicate the process intended for production hardware. In cases where the assembly process involves multiple solder operations (e.g. surface mount reflow, wave solder, rework, hand solder, or conformal coating if used, all these processes must be done on the test assembly. This would be necessary even in cases where only one of the soldering processes is being changed since residues from one process can interact with residues from a prior or following process. It is the total of all these processes that will be shipped and thus it is their total that must be tested and qualified.

NOTE 1: See IPC-9201 for a discussion of the proper methodology and equipment to be usedfor repeatable and accurate SIR testing.

NOTE 2: Keep in mind that the IPC B52 was designed to represent the worst-case conditions for process residue entrapment. Equally, if the user does not employ any through hole connectors, these do not need to be used for this test.

NOTE 3: If the user proposes “press fit” connectors, it is highly recommended that CAF testing be conducted according to IPC-TM-650 Method 2.6.25

5.4 Cleaning

For fluxes requiring cleaning after soldering,clean the test coupons using the cleaning media and method recommended by the flux manufacturer as being suitable for the removal of post-soldering flux residues. Include detailsof the cleaning procedure used on the coupons in the test report.

No cleaning prior to assembly shall be done on the test coupons used in these tests that is not carried out as part of the standard assembly process.

NOTE 1: Consideration of any post soldering manual rework might be an additional process step.

5.5 Coupon interconnection

5.5.1 Connector or Hard Wiring

Methods for connecting test coupons should be by either hardwiring or by connector.

5.5.2 Connector interfacing

Push the test coupon into the edge card connector.

An example of a test set-up using a connector test rack is shown in Figure 5.

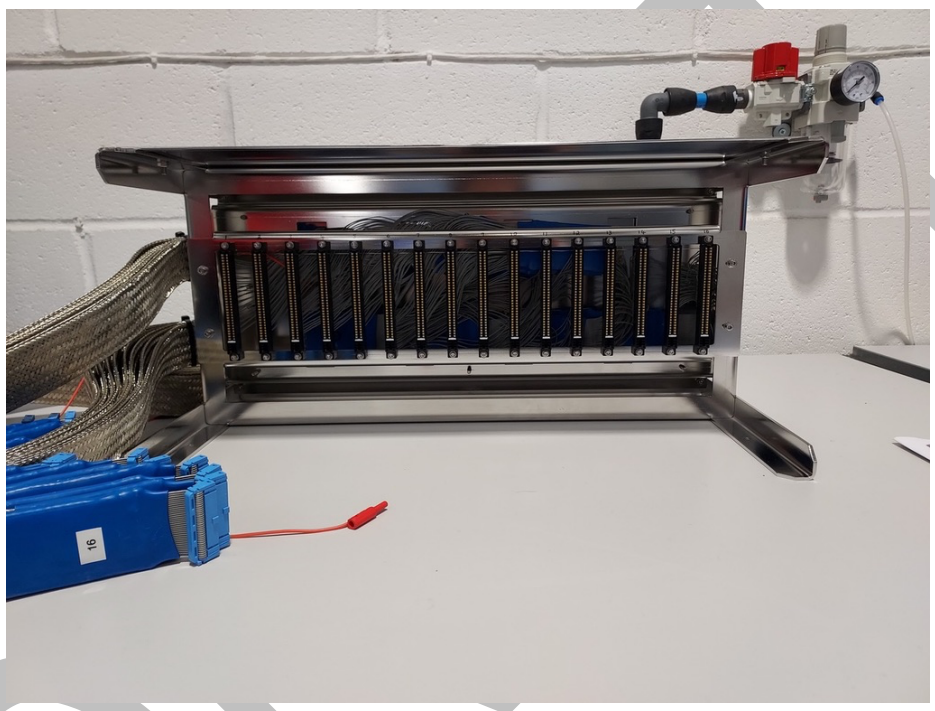

Figure 5: Showing an example of a test rack and showing cable connections.

5.5.3 Connector System - High Resistance suitable for testing between 300V and 1,500V

SIR instruments generally cannot accommodate measurements at voltages above 300V. To extend the range up to 1500V a current limiting resistor is introduced in each measurement circuit. Such a configuration clearly has to be compatible with the various voltage insulation requirements.

Figure 6: Arrangement for testing at voltages up to 1500V.

5.6 Measurement verification

Prior to connecting test coupons to the measurement system, each cable assembly shall be connected to the RVC or Checker Card, inside the humidity chamber that shall be at ambientconditions, and a measurement taken. Any cable that does not read within the tolerance value of the total measurement system as per 3.2 shall be reworked or replaced.

Fixtures shall position coupons uniformly spaced (minimum of 15 mm) andparallel to air flow with the connector (if present), as in Figure 7.

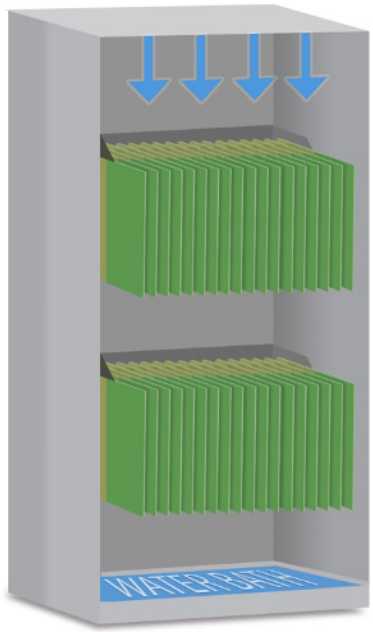

Figure 7: Test Coupon Location with Respect to Chamber Air Flow

6 TEST

6.1 Test conditions

All specimens shall be tested at 40ºC(± 2ºC) with a relative humidity 90% (± 3%) for 168 hours. *The*

IPC committee may wish to add additional environmental conditions.

If the production process involves cleaning the assemblies, then as an alternative,testing may also be conducted at 85ºC (± 2ºC) with a relative humidity 85% (±5%) or AABUS.

It should be noted that modern flux chemistries, especially "no-clean" formulations,use weak organic acids that volatilise easily at temperatures greater than 50 ºC. It is for this reason that it is important to determine the process performance under the worst-case conditions.

6.2 Test Procedure

6.2.1 Insert test coupons into the humiditychamber. If a test rack is used, this shall be already inside the chamber.

6.2.2 Without the bias applied, stabilize the chamber at 25^{0}C/50%RH for 2 hours and takean initial SIR measurement.

6.2.3 Ramp chamber up to test conditions byfirst ramping up the temperature and then the humidity to prevent condensation on test samples. This ramp-up should not exceed three hours.

6.2.4 Apply the bias 1 hour after chamber stabilization at the test conditions. The appropriate bias should then be applied for theduration of the test, except when measurements are taken.

6.3 Test bias

6.3.1 The recommended test and measurement bias is 5V. Alternative bias voltages can be used AABUS. It is important to note that research has shown that lower test voltages are more sensitive to process residues and hence more likely to result in dendritic growth than would occur at 100V. Also note that at 5V, the actual amount of current being drawn is at pA levels and hence EMC and other electrical noise, have more potential to adversely influence measurement results.

6.3.2 Measurement and test bias shall be the same.

6.3.3 Test duration shall be for a minimum of 168 hours. (Note that no-clean material residues are showing electrochemical degradation at durations beyond 500 hours hence a longer test duration is recommended of say 1000 hours.)

6.3.4 Measurements shall be taken at not more than 20 minute intervals.

6.3.5 At the end of the test exposure, removeelectrical bias from all test patterns, prior to temperature-humidity ramp-down initiation.

6.3.6 After ramp-down, stabilize chamber at 25 ºC/ 50%RH for 2 hours and take a final SIR measurement.

6.4 Sample Evaluation

All samples shall be visually inspected at 10X- 30X within 24 hours of test completion and the following conditions recorded:

- Presence of dendrites. If present, record percent of spacing between conductors bridged by the worst-case dendrite.
- Presence of discoloration between conductors (discoloration on conductors only isacceptable). If present, discoloration shall be recorded as a colour image and included in the test report.

- Presence of water spots. If present, these conditions should be recorded as a colour image and included in the test report.
- Presence of subsurface metal migration.When examined with back-lighting, the presence of subsurface metal migration is evidenced by a dark subsurface "shadow" growing from the anode. If present these conditions should be recorded as a colour image and included in the test report.
- Any reason for deleting values (scratches, condensation, solder bridged conductors, outlying points, etc.) must be noted. Rejectionof results for more than 2 test patterns for a given condition shall require the test to be repeated.

6.5 Test Report

The test report shall include, as a minimum, thefollowing information:

The test system report / chart / graph should display the time and SIR values expressed in logohms: e.g. 10^9 LOGΩ. The pass/fail criteria foreach individual process stage would be $<10^8\ \Omega$ However, in assessing the overall process, all results $>10^9\ \Omega$ may be considered acceptable.

NOTE: If the results are consistently $>10^9\ \Omega$ but the trend over the entire test time is degrading,then this shall be construed as a failure.

Details of any post-soldering cleaning procedures employed before coupon conditioning and measurement. Acceptable individual charts or graphs showing the measured resistance include LogΩ vs. time for each coupon and test pattern, or Box plots for the data set; SIR results obtained for each pattern after:

i. Optional preconditioning, if applicable;
ii. Initial, at ambient
iii. Final, at ambient
iv. Any unusual features noted during the test

6.5.1 Examples of failure:

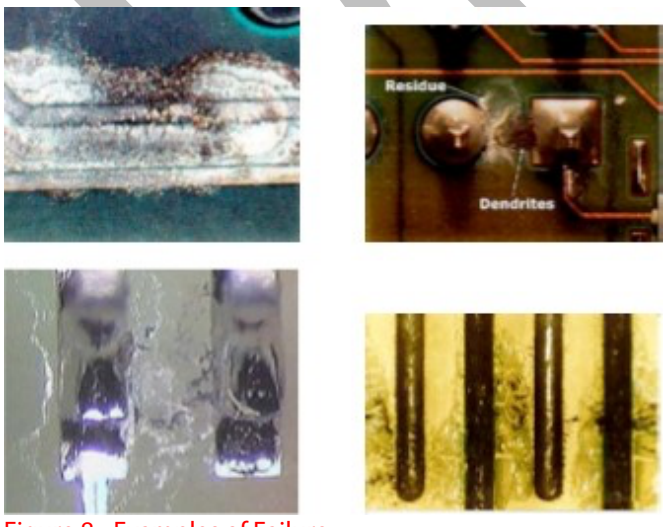

Figure 8 - Examples of Failure

7 NOTES

This annex provides guidance on which test conditions should be used and information on specimen integrity during testing.

7.1 Frequency of monitoring.

During SIR testing resistance values can change rapidly over a period of a few minutes. These are often transitory in nature with SIR values often recovering by the end of the test. Such a drop in SIR may constitute failure in real product. Modern frequent sampling instruments can monitor up to 256 SIR

patterns in less than 20 minutes, and so capture these types of short-lived events. It is recommended that measurement readings be taken as frequent as possible to detect rapid changes in SIR.

If condensation occurs on the test coupons in the environmental chamber while the coupons are under voltage, dendritic growth can occur. Dendritic growth can be caused by a lack of sufficient control of the humidification of the damp heat chamber. Water spotting may also be observed in some chambers where the air flow in the chamber is from back to front. In this case, water condensation on the cooler oven window can be blown around the oven as micro- droplets that deposit on the testcoupon surfaces and cause dendritic growth if the spots bridge the distance between electrified conductors. Both conditions shall be eliminated for proper testing.

7.2 Rain Shield / Drip Shield

It is recommended that a drip shield be placed over and/or around the test samples to prevent water droplets from dropping from the chamber ceiling or from the chamber doors onto the energized test samples. However, the drip shield should also not interfere with good air- flow around the test samples, which may require innovative shielding approaches.

7.3 Electromagnetic Shielding

For consistent and repeatable results, it is important that all cabling carrying test signals be encased in an electromagnetic shield. Most often, this is a metallic foil or braid material.

Since SIR measurement often deals with picoamperes, electromagnetic coupling (EMC) and other stray electrical fields can unduly affect the test signals. Encasing the signal lines with a grounded metal dramatically reduces currents due to EMC and other electrical noise. It is not necessary to individually shield each line, such as in coaxial cabling, but separating voltage supply lines andcurrent-return lines is recommended. A single EMC shield can be used to encase all current- return lines.

7.4 Verification Coupon

During the actual execution of the test program,the verification coupon should be connected to the high resistance measurement system via an external connector or connection. The test coupon can then be periodically measured to verify that the high resistance measurement system is in proper operation condition should anomalous readings be observed.

8 FURTHER REFERENCES

NationalPhysical Laboratory (NPL):