No-clean Flux Appraisal — The Total Process Approach

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ABSTRACT — No-clean flux printed board appraisal tests were conducted with all materials used in the production process. Metallic growths during environmental testing revealed that there was incompatibility between some materials used. Initial tests with two solder resists and several fluxes showed that one non solder resisted board, soldered using a synthetically activated (SA) flux, had surface insulation resistance (SIR) two decades higher than those using low solids flux (LSF) or other SAs. For boards with solder resist, the SIR of those soldered using LSFs was higher, however, than those using SA fluxes.

SIR dependence on temperature and humidity was investigated. Results demonstrated that the dominant factor to determine the SIR of a no-clean board was the characteristics of the board substrate finish. SIR changes with condensation were logged and found to be significant for solder resist finishes. Tests proved that reducing the contamination levels under and on top of the solder resist, by using hot de-ionised water rinsing, enabled the *calculated minimum SIR* level to be achieved for spray fluxed boards and minimised the possibility of metallic growth. Visual examination proved to be at least as important as SIR testing. No-clean processes were appraised using sequential environmental conditions with differing SIR pass levels. As a result of this appraisal a maximum ionic contamination level of 0.5 µg/cm^2 NaCl equivalent and DI water rinses, before and after solder resist added, will be introduced.

Ionic contamination tests indicated that contamination levels reduced with elapsed time, probably due to ionic molecules locking more firmly into the board surface structure.

A novel method for SIR measurements at any voltage,[1] developed by the author, is described. It is hoped that this paper will further the understanding of no-clean flux issues and highlight potential solutions and pitfalls.

INTRODUCTION

With the demise of CFCs for cleaning printed circuit board assemblies, manufacturers are addressing either alternative cleaning methods[2,3] or a no-clean process.[3,4] No-clean has the advantage of reducing the number of production processes involved in PCB assembly and hence cost. Improved process control can be achieved using spray[3,4,5] instead of foam fluxing, reducing the quantity of flux deposited on the board and also removing the concerns of flux contamination and water absorption. No-clean boards subjected in service to either condensing or high relative humidity conditions may cease to function due to electrochemical action causing low SIR, often intermittent, or open circuit conductors. The purpose of the no-clean appraisal carried out by GEC Meters was to determine if this approach could satisfy a long field life requirement of up to 20 years. While a lot of useful world-wide no-clean work has been reported on, the company had reservations about suitable test criteria applicable to this appraisal. Published information[4,6,7,8] appears to indicate that solder flux and resists can be approved in isolation. The approach in this appraisal was that all the materials used in the assembly process should be tested together, because of possible complex chemical interactions exacerbated by high processing temperatures. The test criteria outlined in this paper were arrived at after much initial deliberation and confirmatory testing, which proved invaluable.

SIR MEASUREMENT DETAILS AND PROCEDURE

The measurement circuit is shown in Figure 1. The digital voltmeter (DVM) voltage reading was fed via the DVM RS232 output socket into a microcomputer. The microcomputer prompted for each reading in turn. When the reading was accepted, it was stored in the microcomputer memory, with all test details, including comb reference and resistance in OPS, test temperature and relative humidity, reading duration, date and time. When all the comb readings were completed, the stored results were downloaded into a personal computer and processed on a spreadsheet for graphing. Most DVMs have an internal resistance of 10 MΩ, but the one used in this appraisal measured 11.1 MΩ, as shown in Figure 1. The 56 kΩ resistor, R_S, is negligible, i.e., 0.002%, compared with the 2.6 x 10^9 Ω (1.2 x 10^{12} OPS) 455 squares comb pass limit.

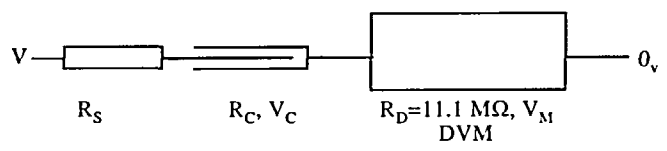

Fig. 1 *SIR potential divider measurement circuit.*

When measurements were not being taken, the DVM was replaced by a shorting link to provide a 60 volt bias to the comb.

where:

R_S = 56 kΩ power supply protection resistor, R_C = Comb pattern resistance
R_D = DVM (digital voltmeter) internal resistance 11.1 MΩ
R_C = Resistance of PCB comb being measured
V = Applied voltage
V_M = Voltage measured using DVM internal resistance
Potential division theorem: $V_M = V[R_D/(R_D+R_C)]$ in volts (1)
Transposes to comb resistance, $R_C = R_D[(V/V_M) - 1]$ in Ω (2)
Comb resistance in ohms per square (OPS):
$\therefore R_C = N \times R_D \times [(V/V_M) - 1]$ in OPS (3)
i.e., SIR in OPS = SIR in ohms x N

where N = number of comb pattern squares = L/D
L = total length of the interleaved comb tracks[9] of opposite polarity
D = gap between comb tracks = dimension of sides of a single square

Also current can be measured down to a level of 1 pA with source voltage up to 1000 V, using this technique, $I = V_M/R_D$.

Calculation of Required SIR Limit

The company's most sensitive circuit uses a device with 0.5 pA maximum offset current. This uses 2 guard tracks, each 25 mm long, separated from the guarded track by 1.25 mm. Potential between guarding and guarded tracks is 15 millivolts.
Number of squares, N = L/D = (2 x 25)/1.25 = 40
∴ Minimum required resistance, R, between tracks:

$R = V/I = 15 \times 10^{-3}/0.5 \times 10^{-12} = 3. \times 10^{10}$ ohms
Minimum required SIR = R/N = 3 x 10^{10}/40 = 1.2 x 10^{12} ohms per square

Measurement Accuracy

At the pass limit of 1.2 x 10^{12} OPS, with 60 volts applied to a 455 square comb the DVM voltage is calculated as follows:

$V_M = V[R_D/(R_D+R_C)] = 60[11.1 \times 10^6/(\{11.1 \times 10^6\}+\{1.2 \times 10^{12}/455\})]$
= 0.25147 volts

Actual voltage applied to the comb = 60 - 0.25 = 59.75 volts
Accuracy of 5½ digit DVM = ±[fsd x 0.019%) + 30 µV] = ± [(0.2 x 0.00019) + 30 x 10^{-6}]
= ±68 x 10^{-6} volts
(fsd = full scale deflection = 200 mV)
Accuracy of voltage reading = ±[68 x 10^{-6} volts/0.25147 volts] x 100%
= ±0.03%
Accuracy of measurement of DVM internal resistance, R_D = ±0.2%
Total accuracy = ±(0.2+0.03%) = ±0.23% OPS (plus normal comb dimension measurement tolerance). Similarly, for 1 x 10^{14} OPS measurement accuracy = ±2.4%.

Basic Measurement Precautions

- As with any SIR high impedance measurement, electrostatic body voltage has an effect, therefore the operator should regularly ground himself to eliminate this effect.
- PTFE cable must be used for acceptable leakage at high temperature and humidity.
- Feed cables from underside of test boards to avoid condensation contamination.
- If the potential division method is used, check that DVM leakage to ground does not adversely affect the measurement; do not rely on the specified CMRR (common mode rejection ratio) — this is measured with 1 kΩ not 10 MΩ across DVM terminals.

BOARDS AND ENVIRONMENTAL TEST DETAILS

Environmental Testing

All boards were subjected to the following *minimum* of sequentially applied conditions:

(i) 7 days at 85°C/85% RH (relative humidity), non condensing, as per IPC-SF-818[7]/TM650 Method 2.6.15 flux corrosion test, but with measurement voltage in same direction as bias. Guideline SIR limit 5×10^{10} OPS minimum.
(ii) 2 days at 40°C/93% RH, non condensing. Calculated SIR limit 1.2×10^{12} OPS minimum.
(iii) 6 days' (24 cycles) cycling between 25°C and 65°C at 93% RH; each cycle of this condensing test was of 6 hours' duration, with 3 hours 55 minutes at 65°C/93% RH. Ramp times of 45 and 60 minutes for rising and falling temperature respectively. Guideline SIR limit 2.5×10^{11} OPS minimum at 65°C/93% RH. SIR readings were taken one to two hours after the temperature had reached 65°C.

This modified IPC-SM-840B[6] test gives an extra cycle per day, longer duration at 65°C/93% RH (IPC specify RH between 90% and 98%) and ramp times 15 minutes less than the specified minimum, to ensure condensation. Test A was conducted at 90% RH. Follow-on cyclic testing at 97% RH revealed that the SIR was an order of magnitude lower than at 90% RH, therefore 93% RH was chosen for all subsequent tests.

Tests 1 and 2 were extended to determine the effect of temperature, humidity and condensation on SIR. For Tests 3 and 4 an additional 40°C/93% RH test was carried out after the cyclic test to check for any change.

Test board coding is defined in Table 1 and the test matrices are given in Table 2.

Test Details

A descriptive summary of the test boards and matrices is given below. All solder resists held IPC-SM-840B class 3 approval. All wave soldered boards had a top side temperature of 105°C, solder wave temperature of 230°C and 2.5 seconds' dwell time. Solder pasted boards were IR reflowed at approximately 210°C for 50 seconds. All boards were fabricated from FR-4 glass epoxy laminate. Eight plated-through hole (PTH) boards in Test 4 were plated to give a 1 ounce finish; all others had 0.5 ounce copper finish. It was originally planned to use 0.32 mm (12.5 thou) comb track width and gap, but it was learned from GPT that they had determined that variable SIR measurements were caused by microscopic solder balling for comb gaps below 0.635 mm. The optimum soldering profile is unlikely to be achieved using a few test boards, therefore the company opted for a nominal 0.635 mm (25 thou) track width and gap for the major test combs. The intention was to test the solder resist and flux as opposed to additional effects from a non-optimised soldering process. The major test combs were based on IPC-25-B,[7] i.e., interdigitated/interleaved comb patterns. The absolute SIR of these patterns was measured in ohms, but to achieve a measurement independent of comb dimensions the unit of ohms per square (OPS)[3] was used throughout.

Test A Board

This test board was for initial flux screening. Test A used single comb boards, with 515 squares, based on the IPC-25-B test pattern with 0.635 track width and gap. A total of 21 boards were tested, 7 with solder resist type 1; 7 with solder resist type 2, and 7 with a bare copper untinned finish, i.e., no resist. Each board type was hand sprayed twice with one of seven fluxes and wave soldered. There were 2 low solids fluxes (LSF)[8] with 3.3% and 4.4% solids, 4 synthetically activated (SA)[5] fluxes with less than 2% solids, and 1 high (15.5%) solids flux (HSF). Only the HSF contained halide at a level of 0.5%.

Tests Board 1 to 4

The company's own test board design, see Figure 2, was used in environmental Tests 1 to 4 to determine the suitability and compatibility of materials for the proposed no-clean soldering processes. Each board comprised the following:

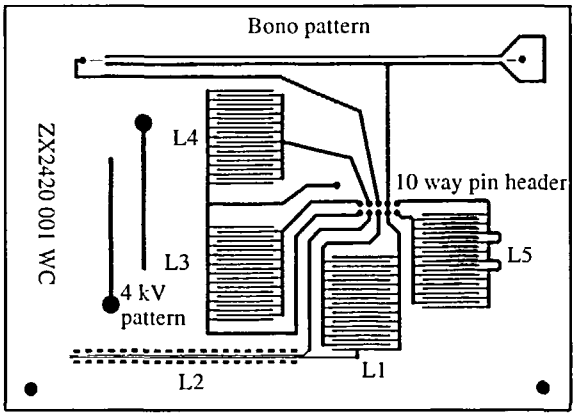

Fig. 2 *GEC Meters' test board.*

Table 1

Test Board Coding

(See Table 2 for 6 Character Board References and Average SIR at 40°C/93% RH)

1	*2*	*3*	*4*	*5*	*6*
Board Finish	*Solder Flux or Paste*	*In House Process*	*Peelable Mask*	*1206 Adhesive or Supplier Process*	*No Clean Wire Soldered Parts*
Code	*Code*	*Code*	*Code*	*Code*	*Code*
1 Resist 1 (PI)	A - Flux 1 (LSF)	A - As received	0 None	0 Not applicable	0 Not applicable
2 Resist 2 (PI)	B - Flux 2 (LSF)	C - Water cleaned	1 Adhesive tape copper film	1 Adhesive 1	1 Connector — using solder 1
3 Resist 3 (PI)	C - Flux 3 (SA)	D - Air dried flux	2 Supplier applied	2 Adhesive 2	2 Connector — using solder 2
4 Resist 4 (PI)	D - Flux 4 (SA)	R - IR reflowed	3 In house applied water soluble	3 60°C DI water rinse, normal processing	3 1206 resistors & connector using solder 1
5 No resist — bare copper tracks	E - Flux 5 (SA)	S - Single comb wave soldered	4 In house applied	4 60°C DI water rinse, processing delays	4 1206 resistors & connector using solder 2
6 No resist — roller tinned	F - Flux 6 (SA)	W - Test board wave soldered	5 Copper tape over connector pads & in house applied peelable mask over 1206 pads & Bono		5 1206 resistors only — using solder 1
7 Resist 5 — two part epoxy	G - Flux 7 (HSF, 0.5% halide)	X - Test board wave soldered and water cleaned			
8 PTH + resist 4	H - Paste 1 (0.25% halide)				
9 PTH: no resist — roller tinned	J - Paste 2 (zero halide)				
	N - None				

PI = photo-imageable solder resist; PTH = plated-through hole double-sided board; LSF = low solids flux; SA = synthetically activated flux; HSF = high solids flux.

Table 2

6 Character Board Test References and Average SIR at 40°C/93% RH for Each Environmental Test

Monitor Board Reference	*Environmental Test A*	*Environmental Test 1*	*Environmental Test 2*	*Environmental Test 3*	*Environmental Test 4*
A	1GS001	5NC001	2BD001	7AW103	6AW031
	12E12	420E12	5.1E12	6.1E12	3.7E12
B	2GS001	3NA001	2CD001	7AW403	4AW031
	1300E12	0.22E12	4.0E12	7.0E12	23E12
C	5GS001	2NC001	2NA001	7AX103	6AW331
	2600E12	1.8E12	7.4E12	10E12	21E12
D	1AS001	4NA001	5CW020	7AX403	4AW331
	1.6E12	2.0E12	470E12	13E12	88E12
E	2AS001	3NC001	4BW020	4NC001	6AW231
	140E12	0.45E12	3.9E12	2.5E12	84E12
F	5AS001	2AW010	5CD001	4AW035	4AW231
	63E12	4.0E12	1200E12	15E12	35E12
G	1CS001	4NC001	4AW020	4AW005	6AW041
	2.1E12	4.6E12	3.4E12	0.35E12	1.2E12
H	2CS001	3AW010	2BW020	4AW035	4AW041
	8.0E12	0.25E12	29E12	10E12	17E12
I	5CS001	5AD001	5NC001	6AX005	6AW341
	45E12	220E12	500E12	150E12	8.9E12
J	1DS001	4AW010	5AW020	4AX005	4AW341
	0.74E12	0.93E12	230E12	6.8E12	160E12
K	2DS001	2AD001	4BD001	4AX035	6AW241
	7.4E12	0.45E12	2.3E12	100E12	80E12
L	5DS001	2BW010	4CW020	7AW504	4AW241
	5100E12	11E12	7.1E12	1.8E12	49E12
M	1ES001	3AD001	4JR001	7AW504	6AW240
	0.99E12	0.094E12	15E12	1.3E12	39E12
N	2ES001	3BW010	2HR001	7AX504	4AW240
	1.9E12	0.22E12	16E12	15E12	76E12
O	5ES001	4AD001	2JR001	6AW103	9AW040
	24E12	0.93E12	7.2E12	140E12	0.037E12
P	1FS001	4BW010	4HR001	6AX103	9AW040
	0.98E12	2.7E12	8.2E12	110E12	0.039E12
Q	2FS001	5AW010	5BW020	4AW133	8AW040
	3.6E12	180E12	260E12	55E12	14E12
R	5FS001	2CW010	5JR001	4AX103	8AW040
	1.1E12	1.5E12	16E12	0.2E12	15E12
S	1BS001	5BW010	4CD001	6AX403	9AW240
	4.8E12	22E12	2.2E12	78E12	0.0053E12
T	2BS001	3CW010	2AW020	6AW433	9AW240
	340E12	0.06E12	5.7E12	3.9E12	17E12
U	5BS001	5CW010	5BD001	4AX403	8AW240
	22E12	180E12	730E12	1.4E12	19E12
V	-	4CW010	5HR001	4AW403	8AW240
		0.7E12	20E12	11E12	28E12

Notes:
1 1.2E12=1.2×10^{12} OPS
2 Values for Tests 1 to 4 are average SIR for comb patterns L1, L3 and L4
3 Tests A, 1 and 2: 40°C/93% RH SIR values measured after 8 days into test cycle
4 Tests 3 and 4 SIR values measured after cyclic damp heat test, i.e., after 16 days' testing.

1 Four interdigitated combs with nominal 0.635 mm track and gap, denoted as L1, L3, L4 and L5. The comb fingers overlapped by a nominal 15.5 mm for each of the 20 'spaces'. Each comb pattern had a measured 455 squares, except for the DI water rinsed batch of boards used in Tests 3 and 4, which had 410 squares. One of these combs, L5, was used for continuous monitoring, via a latching LED circuit with the threshold set at 2×10^{10} OPS minimum.

2 One 3-track comb pattern with nominal 0.3 mm track and gap, overlapping by a nominal 65 mm, denoted as L2. Each comb pattern had a measured 185 squares, except for the DI water rinsed batch of boards used in Tests 3 and 4, which had 167 squares. This pattern was straddled by pads for mounting 1206 size surface mount metal glazed 10 kΩ resistors.

3 One 3-track 'electrolytic cell', for measuring corrosion rate, based on

the Bono principle.[10] This had a 0.13 mm measured average central track and 0.37 mm gaps to the outer conductors.

4 4 kv rms voltage pressure/flash test pattern, with 8 mm between conductors.

The patterns described in 1 to 3 were connected to a specially designed monitor board via a 10-way pin header and PTFE flat cable 1.5 m long. The monitor board accepted up to 22 of these test boards. To prevent the power supply being pulled down by any short circuits, each pattern was protected by individual series resistors on the monitor board, 56 kΩ 0.5 W for the combs and 3.9 kΩ 7 W for the Bono pattern.

Each Bono pattern was continually biased at 60 volts during the environmental test and its central conductor measured before and after to determine any resistance change.

All comb patterns were continually biased at 60 volts during the test, except when individually measured using the same voltage and polarity, with Test A only using a measurement voltage of 30 volts.

Tests 1 and 2

The summarised test matrices were as follows, see Table 1 for board coding and Table 2 for board coded references, with SIR at 40°C/93% RH: Each of the 2 tests comprised 22 boards with the following finishes: Bare untinned (board finish code 5) and three types of 2 pack photo-imageable solder resists, board finish codes 2, 3 and 4. Test control boards, not subjected to soldering, comprised 'in house' water cleaned boards of finish codes 2 to 5 and also 'as received' boards, finish codes 2 to 4. Three fluxes were applied to bare and solder resisted boards using foaming stones, flux codes A and B (LSF types) and flux code C (SA type). Some of these boards were wave soldered and the fluxes on others air dried. For IR reflow soldering, two types of solder paste were applied to some Test 2 boards, codes H and J, both rosin based with the code H paste containing 0.25% halide.

For wave soldered boards the 1206 chip resistors were attached using adhesive code 1 for Test 1 boards and adhesive code 2 for Test 2.

In order to see the variation of SIR with temperature and humidity, Test 1 was extended by measuring the SIR of all boards using three additional environmental conditions. These conditions were 40°C/85%, 60°C/85% and 85°C/93%.

Test 3

The 22 test boards had the following finishes:

- 5 roller tinned boards with no resist, 1 hot DI water rinsed by supplier.
- 10 boards with solder resist code 4, four of these hot DI water rinsed by supplier before and after resist applied. One board water cleaned and used as a control. All DI water rinsed boards handled with gloves by supplier and GECM.
- 7 boards with silk screened 2 part epoxy solder resist code 7; these boards were not DI water rinsed.

Apart from the control board, all were machine sprayed with code A flux and wave soldered.

Other items included in Test 3 were 2 no clean solders and 2 'peelable masks'.

Test 4

Board finish either hot roller tinned solder only or code 4 solder resist, 11 of each. All boards spray rinsed with hot DI water by supplier, as final rinse for bare boards or before and after resist added for resisted boards.

All boards machine sprayed with code A flux and wave soldered. Board supplier applied three different process parameters to the boards used for Test 4; equal numbers of bare and resisted boards were tested:

1 Single-sided — no delay in process before hot DI water rinse — 6 boards
2 Single-sided — process delay before hot DI water rinse — 8 boards
3 Plated-through hole (PTH) — process delay before DI water rinse — 8 boards.

Some boards tested with peelable solder mask code 2 or 3 on the combs. Some board connectors hand soldered using solder wire code 1 only.

TEST FINDINGS

Test A Findings

Table 3 shows SIR values in OPS, at 40°C/93% RH, for the different board finishes and general flux categories; see Table 2 for detailed test results.

The HSF (high solids flux) contained 0.5% halide, but it surprisingly produced the best overall SIR results, with no sign of comb corrosion.

Table 3

40°C/93% RH SIR for Wave Soldered Fluxes and Board Finishes

Board	*Flux Category (Twice Hand Sprayed)*			
Finish	*HSF*	*LSFs*		*SA*
Code	*(Code G)*	*(Code A)*	*(Code B)*	*Synthetically Activated*
1 (resist 1)	12E12	1.6E12	4.8E12	0.74E12 to 2.1E12
2 (resist 2)	1300E12	140E12	340E12	1.9E12 to 8.0E12
5 (no resist)	2600E12	63E12	22E12	*1.1E12 to 5100E12

* The common soldering parameters were lower than recommended by the manufacturer for flux code F only, i.e., lower top board temperature and shorter dwell time in solder, this result being due to unfavourable process conditions for flux code F.

This was attributed to the thick rosin based coating left on the board after wave soldering. This coating not only bonded in the halides, preventing them from taking part in electrical conduction, but also acted as a conformal coating.

The HSF is, however, not suitable for a no-clean process at the author's company because the thick rosin based coating renders it unsuited to automatic test equipment board probing.

For *non* solder resisted boards the SIR of *one* SA flux, code D, was two orders of magnitude higher than the LSFs. The SIR of two other SA fluxes was of the same magnitude as for the LSFs. The SIR of the remaining SA flux, code F, was an order of magnitude lower than the LSFs. All boards were soldered with a common top board temperature and dwell time in the solder, which were both below those recommended by the manufacturer for flux code F only, giving an unfavourable result for flux code F.

For *solder resisted* boards the SIR of the LSFs was at least one order of magnitude higher than for any SA flux. Solder resist 2 had higher SIR than resist 1 for all spray applied wave solder fluxes. Also the SIR of the LSFs was higher than that of the SA fluxes for the resisted boards tested under the other environmental conditions.

Solder resist 2 (board finish code 2) and solder flux codes A, B and C were selected for further testing.

Tests 1 and 2 Findings

Figures 3 to 6 show the variation of SIR with temperature and humidity, obtained by extending Test 1 environmental tests. These graphs demonstrate that the substrate finish, with or without resist, is the dominant factor affecting the SIR of a particular board. Obviously, factors such as contamination or poor curing of the epoxy board laminate or solder resist[11] will also affect SIR.

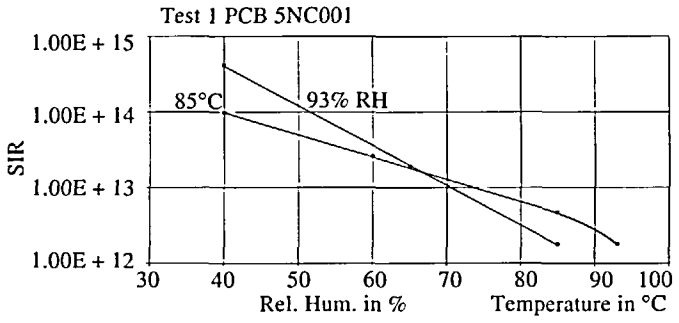

Fig. 3 SIR vs relative humidity and temperature for a water cleaned bare board.

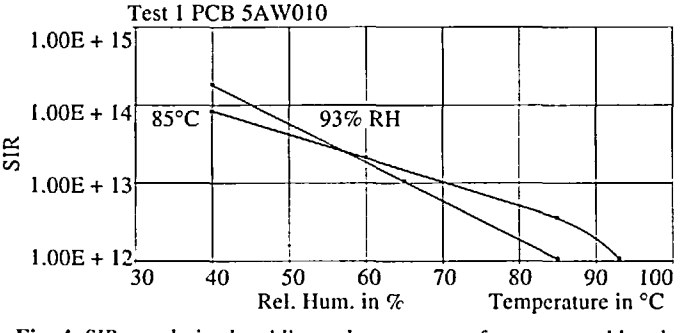

Fig. 4 SIR vs relative humidity and temperature for a wave soldered bare board.

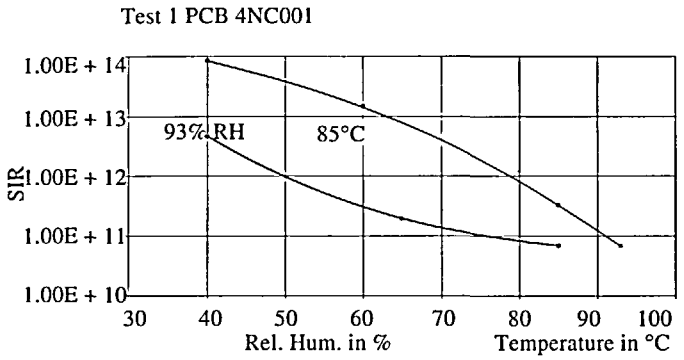

Fig. 5 *SIR vs relative humidity and temperature for a water cleaned resisted board.*

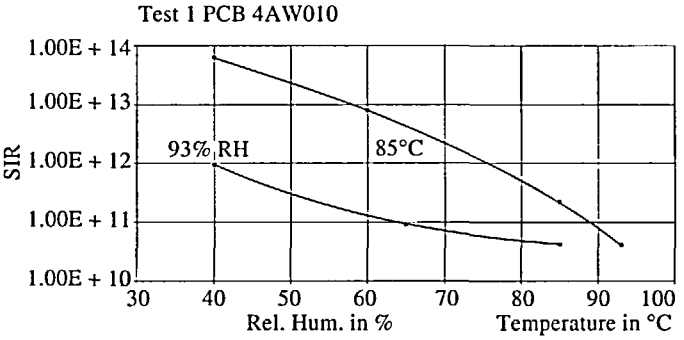

Fig. 6 *SIR vs relative humidity and temperature for a wave soldered resisted board.*

For *non* solder resisted boards, Figures 3 and 4 show that the variation of SIR with temperature at 93% RH is logarithmic. At 85°C the variation of SIR with humidity is logarithmic up to 85% RH. The other two wave soldered fluxes and air dried flux code A exhibited the same relationships.

For solder resisted boards, Figures 5 and 6 show that these relationships are not logarithmic. This was the case for all resisted boards with and without flux added. The variation of SIR with both temperature and humidity followed the same curve patterns for boards with and without added flux.

Board finish codes 2 (resisted) and 5 (no resist), common to environmental Tests A, 1 and 2, were used to compare the 40°C/93% RH SIR of wave soldered boards for both spray and foam applied flux, see summary Table 4. Inspection of Table 4 for *non* resisted boards reveals that the thicker foamed flux residue left after soldering increased the SIR. The SIR of *soldered resisted* boards was reduced by the application of the thicker foamed fluxed and soldered residue. There was little difference in SIR between air dried and wave soldered encapsulating flux types, for individual solder resists; however, investigations by others indicate that this is not the case for *non* encapsulating SA flux types, which were not tested in Tests 1 and 2. Table 5 summarises SIR results for solder fluxed and pasted boards at 40°C/93% RH, in Tests 1 and 2.

Table 4

40°C/93% RH SIR of Spray and Foam Fluxed Wave Soldered Boards

Solder Flux Code	*Board Finish Code*	*Test A (Sprayed)*	*Test 1 (Foamed)*	*Test 2*
A	2	140E12	4.0E12	5.7E12
A	5	63E12	180E12	230E12
B	2	340E12	11E12	29E12
B	5	22E12	22E12	260E12
C	2	8.0E12	1.5E12	-
C	5	45E12	180E12	470E12

As a result of these tests and visual examination, the following combination was chosen as suitable for GEC Meters' use: solder resist code 4, solder flux code A and solder paste code J, the proviso being that further tests, using DI water rinsed boards and sprayed flux, proved that the specified SIR could be consistently met. This was because visual examinations, after environmental testing, revealed blackening of bare copper conductors covered by all solder resist types. This indicated some residual contamination of the board prior to the application of solder resist. Other combinations were deemed unsuitable for the following reasons, referenced to Table5.

Table 5

40°C/93% RH, SIR Summary of Tests 1 and 2 Soldered Fluxed or Pasted Boards and Non-fluxed/Non-soldered Water Cleaned or As Received Boards

Board Finish Code	*Water Cleaned*	*As Received*	*Soldered Paste Code*		*Wave Soldered Flux Codes*		
			H	*J*	*A*	*B*	*C*
2	1.8E12	7.4E12	0.22E12	7.2E12	4.0E12	11E12	1.5E12
	-	-	-	-	5.7E12	-	-
3	0.45E12	0.22E12	-	-	0.25E12	0.22E12	0.06E12
	-	-	-	-	-	-	-
4	4.6E12	2.0E12	8.2E12	15E12	0.93E12	2.7E12	0.7E12
	-	-	-	-	3.4E12	3.9E12	7.1E12
5	500E12	-	20E12	16E12	180E12	22E12	180E12
	420E12	-	-	-	230E12	260E12	470E12

1 Board finish code 3 solder resist could not meet the specified SIR of 1.2×10^{12} OPS; also dendrites[11] were evident on water washed boards, after testing was completed.
2 Board finish code 2 solder resist interacted with no-clean solder wire code 1, used to hand solder the 10-way connector to the board. This caused metallic dendritic growth. Also, the supplier found this solder resist difficult to stabilise.
3 Although solder flux code B gave good SIR results, it interacted with board finish resist code 4 to produce dendritic growth.
4 Solder flux code C caused a considerable amount of white powdery deposits on all resisted boards after environmental testing. It also caused metallic dendritic growths where used in conjunction with resisted board finish codes 2 and 4.
5 Flux paste code H, used with resist board finish code 2, caused metallic dendritic growth.
6 Adhesive code 1 was rejected because it caused copper corrosion, the corrosion being severe enough to cause cracking and lifting of the solder resist.

Tests 3 and 4 Findings

The two part epoxy resin solder resisted boards with finish code 7 were not DI water rinsed by the supplier. The as-received and water finish code 7 boards, hand soldered using no-clean solder wire code 1, had SIR values well above the pass limit. The as-received boards hand soldered using no-clean solder wire code 2 had SIR values around the pass limit and also had metallic dendritic growth on the connector due to interaction between the code 7 resist and solder wire.

Wave soldered, finish code 4/8 boards, which were hot DI water rinsed before and after the application of solder resist, had SIR levels an order of magnitude higher than the calculated minimum of 1.2×10^{12} OPS. Also, blackening of the copper conductors under the solder resist of these boards was eliminated.

Some of the delayed process hot air levelled boards, with no resist, were found to have dendritic growth between test comb conductors after environmental Test 4. This was traced to the fact that this type of board finish, not used at the author's company, was not mechanically scrubbed by the supplier when water washed and went through a heat stoving process before finally being DI water washed. Contamination was therefore baked onto the board.

The average percentage changes in SIR at 40°C/93% RH, for wave soldered boards using code A flux, following the damp heat cyclic test, were as follows:

2 part epoxy resist, board finish code 7, not DI water rinsed: +12%
2 pack photo-imageable resist, board finish code 4, not DI water rinsed: -66%
2 pack photo-imageable resist, board finish codes 4 and 8, DI water rinsed: -24%

Figures 7 and 8 show the difference in SIR after the damp heat cyclic test for finish code 4 solder resist, wave soldered using code A flux. Figure 8 is for a board which was hot DI water rinsed before and after solder resist added.

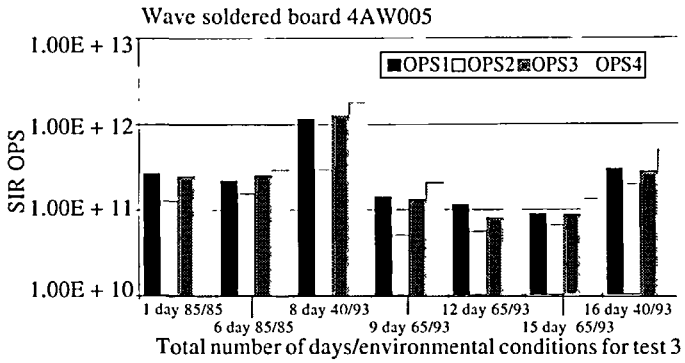

Fig. 7 *SIR of a wave soldered, solder resisted board for environmental test 3.*

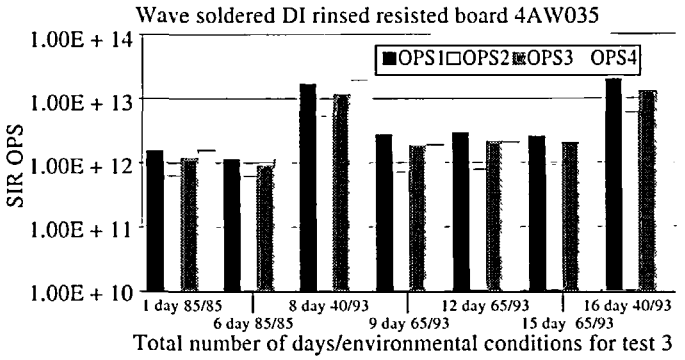

Fig. 8 *SIR of a wave soldered, DI water rinsed, resisted board for environmental test 3.*

Table 6

Bono Resistance Changes — Wave Soldered Boards

Env. Test Number	*Board Finish Code*	*Change in Resistance Ave. %*	*SD %*	*Comment*
1 & 2	5	0.8	-	not tinned or solder resisted, water washed
1 & 2	5	1.8	-	not tinned or solder resisted
1 &2	4	1.7	0.4	PI solder resist 4
1 & 2	2	3.2	1.2	PI solder resist 2
1 & 2	3	3.8	0.6	PI solder resist 3
3	7	2.2	-	2 part epoxy resist 5
3	4	0.1	-	DI rinsed, PI solder resist 4
3	4	0.7	-	PI solder resist 4
4	4/8	0.5	0.3	DI rinsed, PI solder resist 4
4	4/8	0.6	0.2	DI rinsed, resist 4 — supplier masked
4	4/8	0.5	0.0	DI rinsed, GEC masked/water washed
4	6/9	1.4	0.2	DI rinsed, tinned/hot air levelled, no resist
4	6/9	1.3	0.7	DI rinsed, tinned & supplier masked
4	6/9	1.4	0.1	DI rinsed, GEC masked & water washed

Note: Worst case tolerance for each measurement of nominal 1 ohm tracks (PTH 0.5 ohm) was ± 0.2% of reading, ∴ tolerance for resistance change ± 0.4%.

Table 7

Board Supplier's Water Wash Bath Analysis

Chloride (total as chlorine)	: 161 mg/litre
Copper (as copper)	: 113 mg/litre
Lead (as lead)	: 0.4 mg/litre
Fluoride (as fluorine)	: 0.3 mg/litre
Iron (as iron)	: 0.3 mg/litre
Tin (total as tin)	: 0.2 mg/litre
Chemical oxygen demand	: 20 mg/litre

Contamination Tests

Ionic contamination measurements for various boards, as received from the supplier, are summarised in Table 8. These are the calculated asymptote values, with measurement times of up to 15 minutes. All measurements were at ambient temperature using equal proportions of isopropyl alcohol and de-ionised water to dissolve the contaminants. The majority of boards had contamination levels below the generally accepted, but lately questioned 1.5 µg/cm^2 (NaCl equivalent). The exceptions to this were boards handled by the supplier without using gloves. Most were still 'leaching' at the end of the measurement period, although all board finishes had zero ionic contamination if in-house water cleaned before measurement.

Table 8

Contamination Test Results in µg/cm^2 for Unprocessed Boards

Env. Test No.	*Test Delay in Weeks*	*Board Finish Codes*						
		Bare		*Solder Resisted*				
		5	*6/9*	*1*	*2*	*3*	*4/8*	*7*
A	1	1.0	-	0.4	0.5	-	-	-
1/2	3	0.6/0.6	-	-	1.1/1.1	1.2/2.4	0.7/1.2	-
3 ∇	1	-	2.2/2.9	-	-	-	0.9/1.2	0.9/0.9
3 *	1	-	0.9/1.0	-	-	-	0.5/0.5	-
3 *	21	-	0.12/0.15	-	-	-	-	-
4 +	12	-	0.15/0.2	-	-	-	0.04/0.06	-
4 *	12	-	0.04	-	-	-	0.04	-

∇ = Supplier DI water rinsed, boards handled without gloves
* = Supplier DI water rinsed, boards handled using gloves
\+ = Supplier process delays, DI water rinsed, boards handled using gloves

Boards processed for use in environmental Test 4 had lower contamination levels than expected. These boards were measured 12 weeks after receipt, therefore a reduction in measured level with elapsed time was suspected. To check for this, two further boards processed for use in Test 3 were measured 21 weeks after receipt. The measured levels were between 13% and 17% of those for similar boards measured 1 week after receipt. These results indicate that some of the ionic contaminants may have locked more firmly into the board surface structure with elapsed time.

Board Supplier's Water Bath Analysis

Six water wash baths used by the blank board supplier were analysed by their local water supply authority; see Table 8 for the worst bath, used for washing PTH boards. Some of these elements such as chlorine and fluorine are present in the water supply, but were concentrated by washing bath 'carry over'. The water bath analyses backed the conclusion prior to Tests 3 and 4 that DI water rinses were required to obtain the calculated SIR level with minimum risk of electrochemical action.

Bono Based Corrosion Rate Resistance Test

This test,[10] which needed great care, using 4-terminal measurement and correction for the resistance variation of copper with temperature, does appear to be useful. It showed up relative differences in the corrosion rates of solder resists used in Tests 1 and 2, see Table 6. The resist with board finish code 4 had a corrosion rate roughly one half of the other two, codes 2 and 3. The corrosion rate for DI water rinsed, code 4/8 resist, in Tests 3 and 4, was shown to be substantially reduced at 0.1/0.5%, compared with 1.7%. This would have been expected to be roughly halved, without DI water rinsing, because the environmental test time was not extended as for Tests 1 and 2. A lower corrosion rate for code 4 resist was obtained in Test 3 than in Test 4; differences in hand pumped spraying and temperature of the DI water used for the two test board batches may have affected this.

This method, however, did not indicate the propensity of the delayed process (Test 4), hot air levelled, non resisted boards with baked-on contaminants, to dendritic growth, when compared with Tests 1 and 2 untinned non DI rinsed boards.

Effect of Condensation on SIR

The temperature cycle used to induce condensation is described in Environmental Testing Section (iii). Refer to Figures 9 and 10 which show changes in the logged voltage, measured at one minute intervals, for comb L1 of each board during Test 2. These show typical results for solder

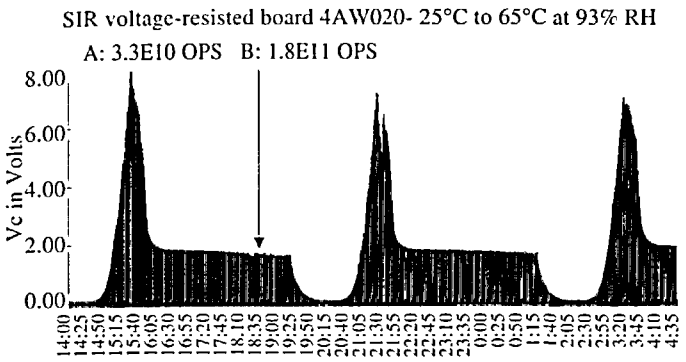

Fig. 9 *Variation of comb voltage with condensation for a wave soldered, solder resisted board.*

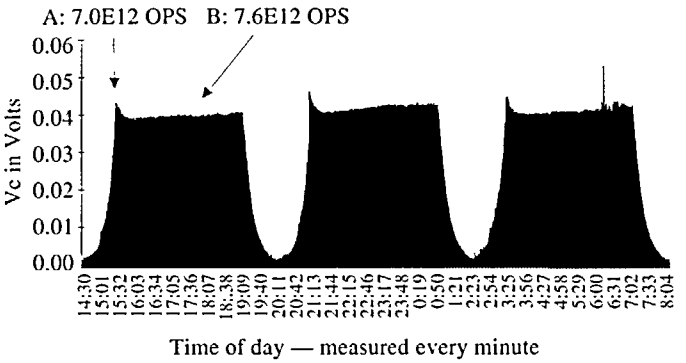

Fig. 10 *Variation of comb voltage with condensation for a wave soldered bare board.*

resisted and bare untinned soldered finishes. The comb voltage was graphed because it is easier to see the relationship with the temperature profile; the SIR is calculated as in Equation (3), which follows the Introduction. The portions of the graphs close to zero show the comb voltage measured at 25°C/93% RH. As the temperature rises from 25°C to 65°C, condensation occurs and the voltage is seen to overshoot at A, 65°C/93% RH. The condensation gradually disappears and the voltage is relatively stable at B, 65°C/93% RH, during a period of approximately 3 hours, before the temperature was reduced to 25°C again. Figure 9 shows that condensation on this solder resisted board caused the SIR to fall to 18% of the stable value at B, 65°C/93% RH, i.e., from 1.8×10^{11} to 3.3×10^{10} OPS. Figure 10 shows that the untinned non solder resisted board, condensing SIR, only fell to 92% of the non condensing stable value at B, 65°C/93% RH, to 7×10^{12} OPS.

The reduction of SIR with condensation for boards, either solder pasted/IR reflowed or with foam applied air dried flux, was less than for as-received or water cleaned boards, of the same type finish. This appears to be due to the encapsulating rosin acting in a similar way to conformal coating.

The SIR reduction with condensation for foam fluxed wave soldered boards was a little more than for as-received or water cleaned boards with the same type finish. This is probably due to long chain molecules with free water attractive ionic links being formed during the wave soldering process.

Voltage Pressure (Flash) Test

This test was carried out on boards after recovery from the environmental tests. The minimum withstand voltage of the 4 kV test pattern was 5.5 kV rms for 1 minute.

CONCLUSIONS

This appraisal demonstrated that the substrate finish is the dominant factor which affects SIR and that complex chemical interactions make it necessary to check combinations of all the materials used in a no-clean process in order to avoid costly field failures. Condensation was shown to affect the SIR value of *solder resisted* boards considerably. The cyclic damp heat test was useful for promoting potential electrochemical action. Also, a comparison of the SIR at 40°C/93% RH before and after this test was particularly informative. It is the author's view that it is safest to use a rosin/resin based low solids flux/paste for a no-clean process, since this addresses to some extent, by encapsulation, the potential problems of halide contamination on components and printed boards (flame retardant bromines etc.). These halides should become bonded into the rosin matrix, thus preventing ionic conduction. It is important, however, to ensure that bare boards are correctly cured, cleaned and handled, in order to minimise the possibility of electrochemical action.

As a result of this appraisal, a single combination of materials only was chosen for the no-clean process. This was board finish code 4 solder resist, wave solder flux code A, reflow solder paste code J and no-clean solder wire code 1. The company is confident that the reliability of its assembled boards, produced using this combination, along with improved processing and handling, will be higher than for boards using the current water cleaning process with hot sprayed DI water. Production batches using the chosen no-clean materials combination have not caused any problems with automatic test equipment probing. However, precautions have been taken such as masking sockets from the effects of the sprayed flux. The bias voltage gradient for the larger combs with 455 squares was 95 volts per millimetre, while present worst case applications use 50 V/mm. The author believes that it is important to use similar bias and measurement voltages[1] and also realistic voltage gradients. This improves measurement accuracy,[1] with the added benefit of much shorter test times due to improved SIR stability. Negligible difference was found in test time or SIR value when using measurement voltages of 30 V and 60 V with a same polarity bias of 60 V. Use of reverse bias measurement voltages did affect stability, such that several minutes, instead of seconds, were sometimes required, particularly for bare boards.

The temperature and humidity were also independently monitored, such that it was possible to see quick and significant SIR changes with the occasional ±1% RH changes as the humidity chamber maintained control. Figures 3 to 6 indicate SIR changes which may be expected if a chamber with an uneven temperature/relative humidity is used to provide the environmental test conditions.

The company will continue to use sequential environmental SIR testing for further qualification testing, with the same pass limit at 40°C/93% RH. In addition to setting a contamination level of 0.5 $\mu g/cm^2$ maximum for incoming blank boards, GEC Meters/supplier will monitor the SIR of control test boards produced with each batch. It is also intended to monitor and set contamination level limits for assembled no-clean boards as part of process control checking. Contamination testing should not be treated as proving definitively that a board is clean. It is a good indicator of the *average level* of ionic contamination on a board, but it should be appreciated that small areas with a relatively high contamination level may cause electrochemical problems. Also ionic contamination levels appear to reduce with elapsed time. There is no substitute for good board processing and handling to avoid such problems.

Future testing will be improved by the use of the 'carrier material' only for solder pastes, to avoid potential damage to solder resist on removal of large reflowed solder balls from it. If the author's company carries out any further adhesive tests, the adhesive will be spread over combs to obtain true SIR values, not 'spotted' over a comb as in this appraisal. There was initial surprise that *non* resisted, untinned boards, and also tinned boards with no process delays, did not grow dendrites during the cyclic damp heat test. It was later appreciated that processing problems and poor cleaning are probably the causes of the problems reported by some for this type of finish.

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continued on page 32

evaluations and second, boards have components at locations far away from the feeder.

Efficiency loss due to board transfer:

The overall transfer time range for surface mount PCB assembly equipments is 4 to 15 s.[12] This will be a significant factor in the case of small batch size.

Therefore the corrected throughput (t) is:

$$t = R_b \times Avail \times Util \times Effi.$$

Throughput Rate

The throughput rate is determined by first identifying the bottle-neck of the facility (machines whose capacity is lower than that of the demand). The bottle-neck is going to be dependent on the PCB. The throughput rate of the bottle-neck machine will determine the throughput rate of the assembly line.

SYSTEM INPUTS AND OUTPUTS

Inputs can be provided to the cost advisor and the DFM environment in two different formats at two stages of the PCB design process. At the initial stage, while designing the circuit before creating a schematic and defining the board size and shape, the designer uses list boxes and interactive methods to provide a standard board size, components and materials required to manufacture the board. The system then calculates a rough assembly cost from the selected inputs. The design advisor can receive input from a CAD drawing in the form of a .dxf file format. At this stage, the design is typically complete, and the PCB is being sent for fabrication. The system extracts relevant information from the CAD .dxf file such as board dimensions, component types, their number, location and orientation of the components on the PCB, etc. The output of the system consists of a micro process plan, assembly/manufacturing cost of the given PCB, and the throughput rate for a given PCB.

CONCLUSION

The design of a PCB significantly influences its assembly cost. It is therefore important to provide the designer with decision support tools which will help in lowering product cost. Advances in SMT including ultra-fine pitch components, multilayer boards, increased board density, enhanced production rates, shorter product life cycle and high yields mandate the use of DFM principles. This paper describes a cost estimator tool that would present the manufacturing/assembly cost to the designer during the conceptual design phase. The cost analysis can be best applied as an aid for designers by providing rapid comparisons at an early design stage. The system described uses a knowledge based framework. Object oriented programming techniques were used to develop the system. The main advantage of using this approach is that it allows for a step-wise, modular development of the system.

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continued from page 27

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