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Test Procedure for Process Validation using Surface Insulation Resistance

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ABSTRACT

Surface Insulation Resistance (SIR) testing uses a test circuit with a comb pattern design to which a bias voltage can be applied, and leakage current measured. The effects of voltage and combs patterns pitch are critical to the behaviour of process residues and their effect on SIR. Calculations assuming homogeneous sheet resistance and electric field are not valid and cannot be used to predict the performance for electronic devices with differing geometries.

This work shows that electronics manufacturers measuring the effect of process residues must consider the geometries of the SIR test sites, which need to be representative to produce meaningful SIR data.

Furthermore the reality of the production process for a typical printed circuit assembly (PCA) leaves residues from numerous chemical processes, not just the soldering flux. In order for the potential impact on reliability for all of these to be assessed a test vehicle should be used and prepared via the production line of interest.

This report outlines a procedure for the validation of an electronics manufacturing process using SIR. It offers guidance for the design of test vehicles appropriate for production processing. SIR data collected using this procedure is more representative than that based on flux qualification.

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Approved on behalf of Managing Director, NPL, by Dr C Lea,
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1. Introduction

Surface Insulation Resistance (SIR) testing uses a test circuit with design of two interdigitated comb patterns to which a bias voltage is applied. The comb pattern simulates the conductor traces on circuit boards and following processing leave residues on the comb patterns. The test vehicles are subjected to elevated temperature and humidity conditions to promote corrosion, current leakage and electrochemical growth that are measured via changes in resistance between the comb tracks. Low SIR is indicative of harmful residues likely to lead to poor reliability of electronic product in the field.

Historically SIR has been used to qualify flux materials for use on printed circuits using a standard test vehicle with single comb geometry. However, recent studies by NPL [1] have shown that the effects of voltage and pitch of combs patterns are critical to the behaviour of residues and their effect on SIR. It has been shown that calculations, which endeavour to relate results from different comb pattern geometries by assuming homogeneous sheet resistance and electric field, are not valid. For a user of flux or paste materials this conclusion means that the geometries of the components used in printed circuit assemblies (PCA's) need to be represented for the results to be meaningful to their product.

Furthermore the reality of the production process for a typical printed circuit assembly (PCA) leaves residues from numerous chemical processes, not just the soldering flux. In order for the potential impact on reliability for these to be assessed a test vehicle that lends itself to preparation via a production line is needed.

This report outlines a procedure for the validation of an electronics manufacturing process using SIR. An example of a test board design is given, which is representative of a PCA. It has components mounted and soldered onto it, and can be passed through the processes needed for surface mount manufacture. SIR data collected from this design will be more representative since the residues will be the same as those on PCA's coming from the production line, and the SIR response is relative to the electrical conditions on the PCA.

2. Test Board Design

The choice or design of your test vehicle is critical to achieving valid measurements. The component types and geometries must be as close as possible to those used in your actual manufactured electronic product. This is because:

- Different pitch geometries give different SIR data, even when the same voltage gradient is applied
- Different component designs have a different propensity to trap/localise process residues

It is necessary to ensure that dummy components are available for your design. They must be isolated dummy components, with no internal die or functionality. Scrap devices subsequently sold as dummies will often allow current flow between the component leads invalidating SIR measurements. This requirement must be stressed to the component supplier. For chip components using low value capacitors with the same geometry, rather than resistors, is necessary.

If your product is manufactured with mixed technology, then your test vehicle should be capable of processing in this way, with test sites on both sides of the board.

For multi-layer boards it is not necessary to build a multi-layer test vehicle. The SIR test examines surface leakage and electrochemical corrosion mechanisms. Using a single or double-sided test vehicle reduces costs. If you are concerned about sub-surface failures then a different approach is needed [2].

An example test vehicle for SIR process validation is shown in Figure 1. The design includes array devices (BGAs, mBGA and a flip chip), QFPs, and discrete devices. This test vehicle was designed for NPL evaluations.

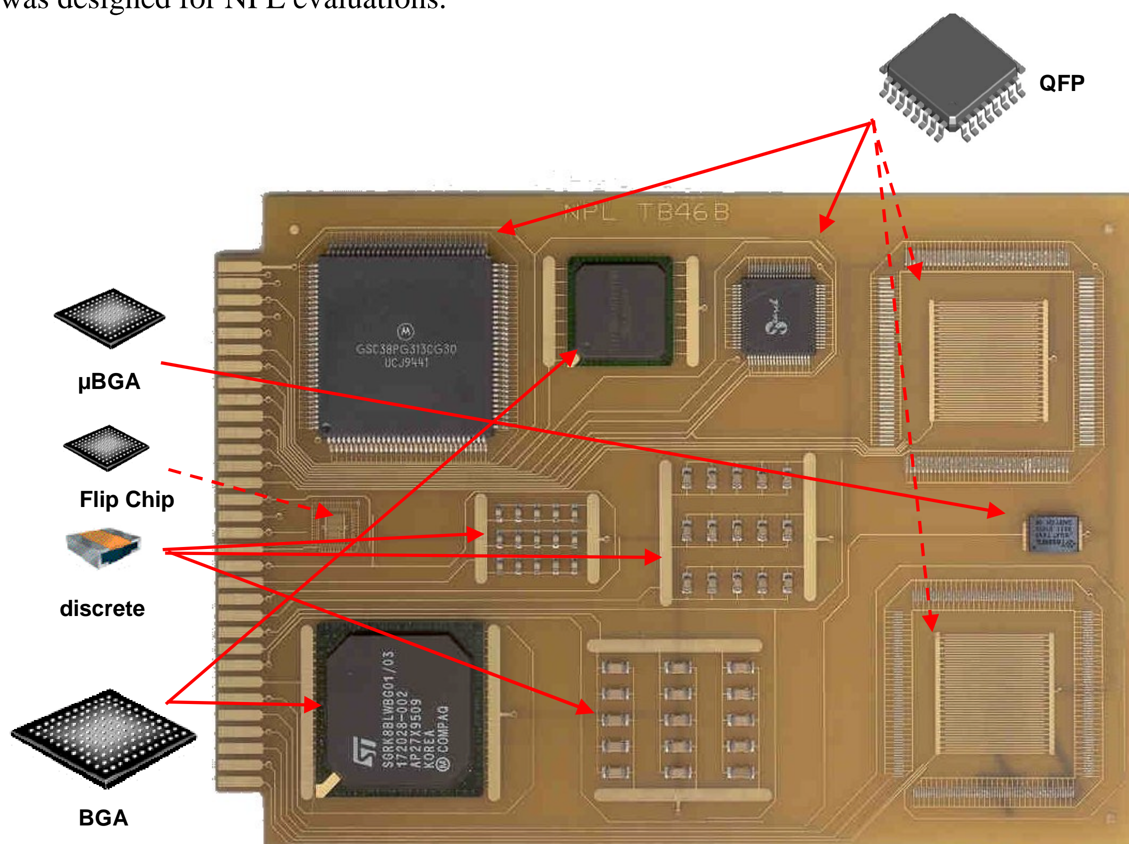


Figure 1. SIR Process Validation Test Board TB46 – Surface Mount Demonstrator

2.1. *SIR test sites – The Comb Pattern*

The simplest set site for an SIR measurement is shown in Figure 2.

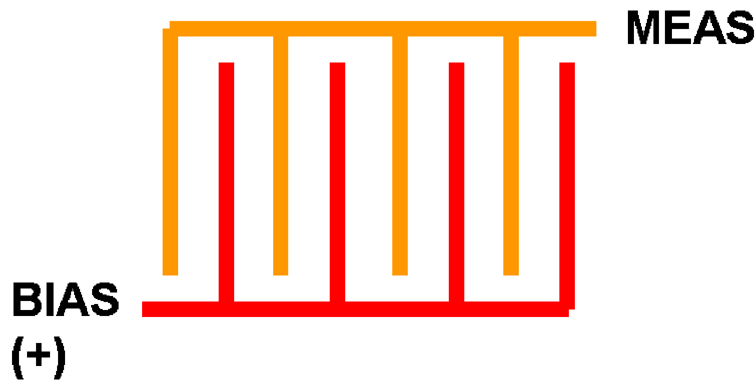


Figure 2. Schematic of basic comb pattern

The bias track is held at a positive voltage, the measurement track is the point at which any leakage current flowing is detected. In addition to bias and measurement tracks, ground tracks can also be used on test vehicles. These tracks are used in-between the bias and measurement tracks at points outside the areas of interest. They prevent current leakage between adjacent measurement circuits.

All SIR test sites (or combs) are based on this basic principle, although the layout must be optimised for each component type.

It is pertinent to consider the specific board layout design rules when preparing the Gerber for your test vehicle. For example, if your design rules allow for tracks to pass between QFP and BGA pads at a certain pitch this should be applied to the test patterns too. You should make pad and stencil aperture sizes in line with design rules so that pad gaps and solder paste volumes are correctly represented. If solder resist is included as part of your processing options then, again, design rules should be followed (with some exceptions, see section 2.2).

2.2. SIR test sites for QFPs

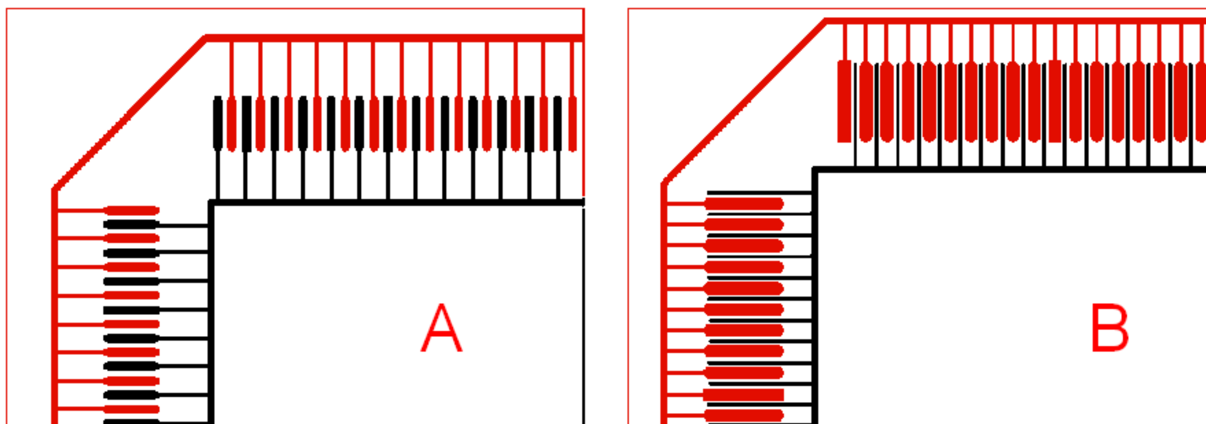


Figure 3. Alternative comb designs for QFP devices

Figure 3A shows the simpler comb pattern design for SIR testing with QFPs. Each alternate pad is connected to a bias voltage. The other pads are used for measuring any leakage current. Figure 3B, however, shows a design suitable for cases where design rules allow traces to pass

between QFP tracks. Here every pad associated with a QFP lead has a bias applied to it. The interleaved traces are used to detect leakage currents.

Note. This has two important effects:

i) It dramatically reduces the effective pitch and gap
ii) It removes the necessity for the internal connections of the QFP to be isolated

Comb patterns can be placed beneath the QFP area if desired. These combs will detect any residues that are trapped under the low stand off component. They are particularly useful for SIR trials that include cleaning steps, as this is an ideal trapping zone for wash rinse residues. If testing sites beneath a QFP to detect residues this should be kept free of solder resist.

2.3. SIR Test Sites for Array Devices

For array devices a very straightforward comb design can be used as shown in Figure 4A, where the bias and measurement tracks are associated with the solderable pads for the package. For those designing product with tracks running between BGA/CSP pads, however, a design similar to Figure 4B would be more suitable. Here all the pads are held at the bias voltage with interposing measurement tracks.

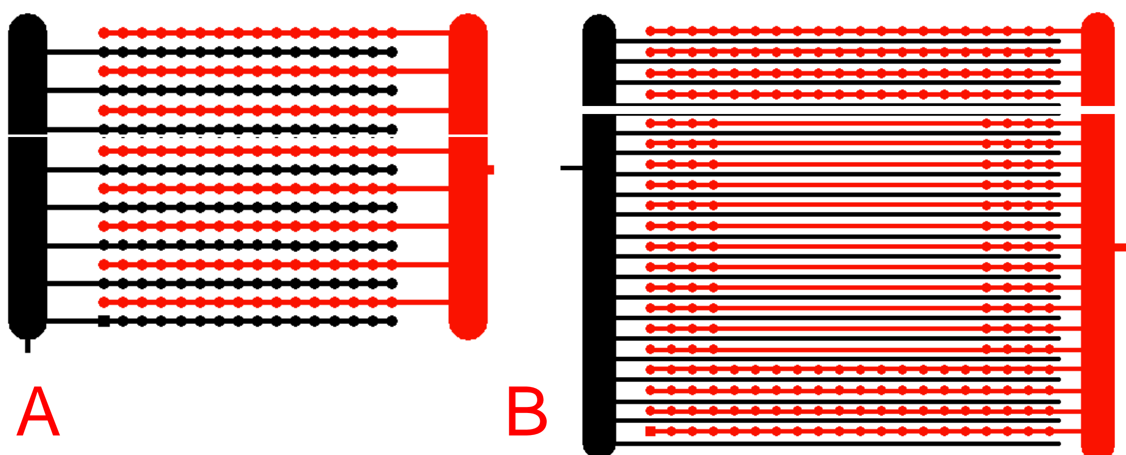


Figure 4. Alternative comb designs for array devices

2.4. Chip Components

Chip components are particularly prone to trapping residues under the low standoff area between pads. The SIR test site design for these devices is uncomplicated, utilising the pads for the application of bias and taking the current flow measurement between them. This approach is of course only valid for measurement of DC resistance with capacitors.

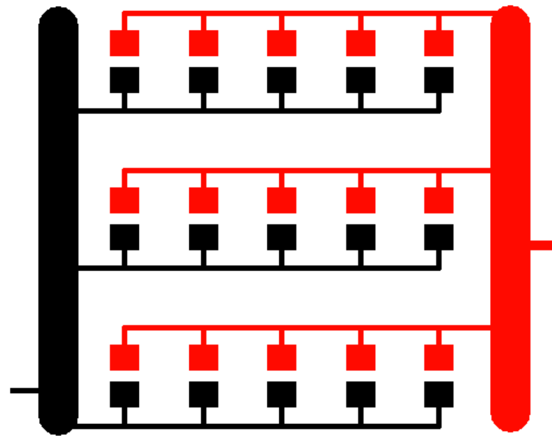


Figure 5. SIR test site design for chip components

For larger chip components where design rules may allow tracks to run between pads this can be represented in the design.

3. Identifying the process steps

The process manufacturing steps to be represented in the test need to be identified. Each process should be represented in the test matrix. A typical test matrix is shown in Table 1. The seven steps are suggested as a sensible breakdown of the assembly process. Different processes are applied to each sample coupon, represented by the crosses in Table 1.

The sequential approach of the experiment can be seen, which helps when analysing the results. For example, if poor results are seen for coupons 13 and 14 it suggests that contamination is being introduced through the cleaning process. It should also be noted that some coupons are to be processed with wave flux, or paste alone to separate the effects from each.

Table 1. Example of processing plan for test coupons in order to represent a production process

Process	Coupons							
	1,2	3,4	5,6	7,8	9,10	11,12	13,14	15,16
PWB solderable finish	x	x	x	x	x	x	x	x
Solder Resist		x	x	x	x	x	x	x
TH Component Place + Wave Solder			x		x	x	x	x
Solder Paste				x	x	x	x	x
SM Component Place & Reflow						x	x	x
Cleaning Media							x	x
Conformal Coating								x

This matrix is only meant to serve as a example, in practice the matrix can be suited to the areas of interest for each case. Some users may choose to have more than one surface finish, paste, flux, resist or even coating in the matrix in order to select the best performing.

4. Processing the Test Vehicles

The test vehicles will model the assembly as closely as possible, and it is important to ensure the same is true for the processing of them. Parameters such as reflow profiles, belt speeds, temperatures etc, should all be those intended for production. This eliminates as far as possible any effects caused by differing parameters.

The parameters used should be recorded, and as a minimum those suggested in Table 2 can act as a guide. Since changing these parameters can affect the SIR results obtained it is important to note them.

Table 2. Guide to process parameters

	Parameters to Record			
PWB solderable finish	Type	Bath Time/Temperature	Finish Thickness	
Solder Resist	Type	Development Profile	Cure Profile	Thickness
TH Component Place + Wave Solder	Flux Type	Belt Speed	Thermal Profile	Wave Temperature
Solder Paste	Paste Type	Stencil Thickness	Squeegee Pressure and Speed	
SM Component Place & Reflow	Belt Speed	Reflow Profile	Oven Settings	Atmosphere
Cleaning Media	Type	Immersion/Spray	Time/Temperature	Ultrasonics
Conformal Coating	Type	Dip/Spray	Cure Conditions	Thickness

5. Analysing SIR Data

For steady state exposure of SIR samples a typical response with time is shown in Figure 6.

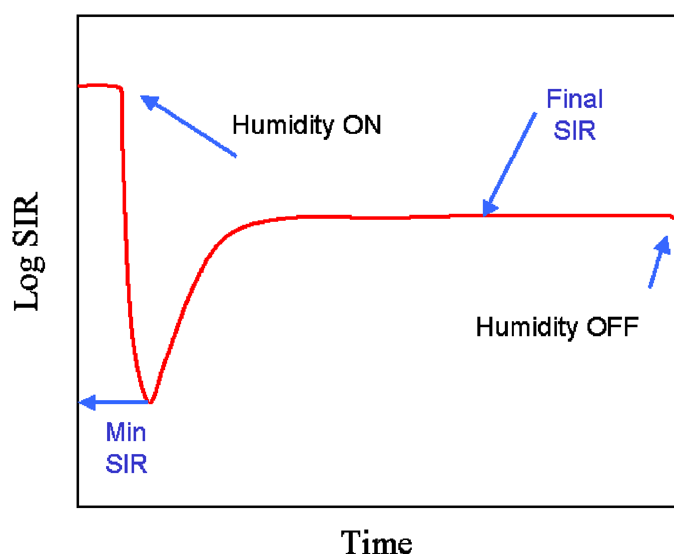


Figure 6. Schematic of SIR time plot

The resistance of the samples drops as humidity fills the chamber and penetrates the samples. The initial SIR is generally lower than that once the system has stabilised due to ‘sweeping’ of ionic species across the surface. The value of interest is the final, stabilised, SIR reading. Although time consuming this value is best acquired by examining plots individually. If an algorithm is used to try and ascertain the value important information can be missed. Dendritic growth is a crucial example, as shown in Figure 7. Samples with dendritic growth can recover to high SIR values later in the test time, and so a visual examination of the results is advised rather than on numerical data from an interpretation algorithm.

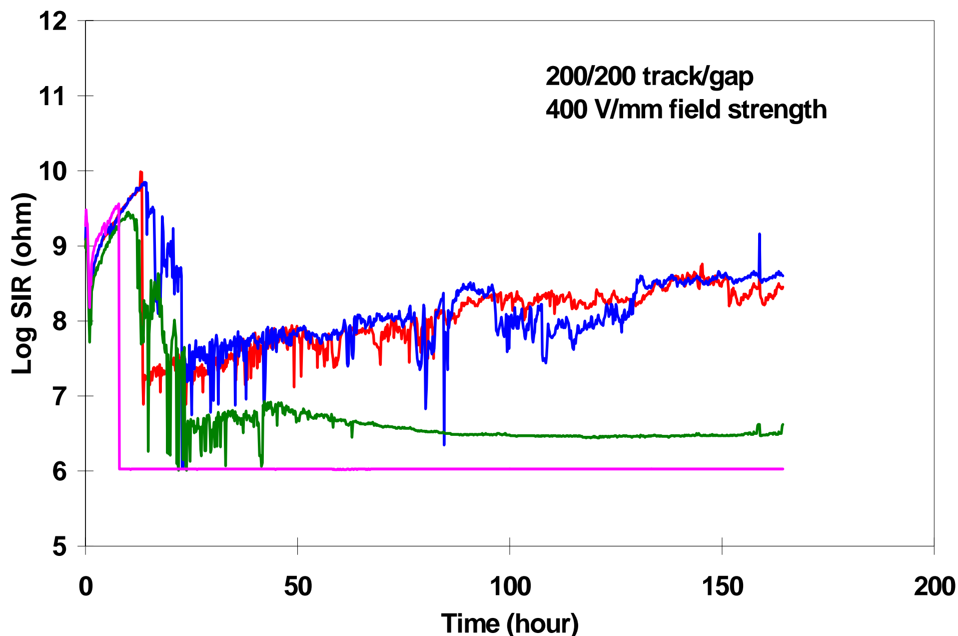


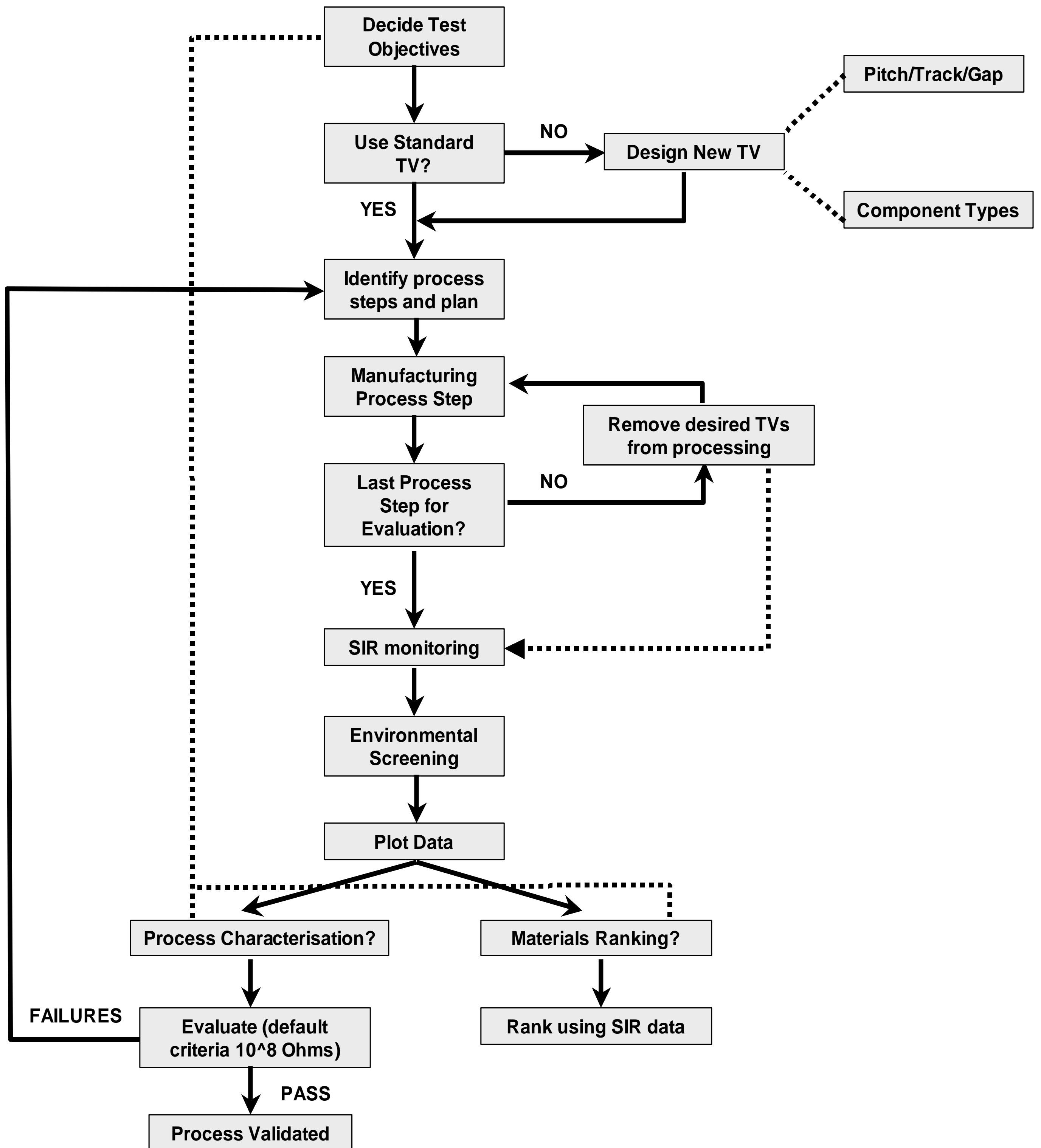
Figure 7. SIR time plots showing dendritic growth behaviour

Higher SIR values are favourable, with low SIR being indicative of poor reliability in the field. Be aware of the effects of your test site design on the result obtained. Certain designs (fine pitch, low stand off, large number of tracks) will be more prone to leakage and dendritic growth.

Do not attempt to correlate results from different geometries by using the ‘ohms square’ approach, which assumes uniform surface resistance. This has been shown to lead to false assumptions.

When considering the implications of low SIR readings for a particular device, residue or process, ideally try and consider the reduction in insulation resistance that would affect the function of the electronic product(s), in question. This data is not always readily available, and so it is wise to also include in your study a control process. A good example of this would be a standard tin-lead based soldering process, which has been used historically, and for which you have a history of product performing reliably in the field. Processing coupons with this existing ‘high confidence’ process alongside the new processes on trial allows comparison to a reliable reference.

6. Procedure Schematic



7. Acknowledgments

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8. References

1. NPL Report - MATC(A) 70 ‘Development of Surface Insulation Resistance Measurements For Electronic Assemblies’, Christopher Hunt
2. See ‘Conductive Anodic Filamentation Testing’ at www.npl.co.uk/ei/services